Directions

Exit Aachen-Laurensberg

Düsseldorf A44 ✈

Direction Heerlen

Köln A4 ✈

Kohlscheider Str.

Lüttich A44 ✈

Toledo Ring

Extension Building of the IT Center

Melaten RWTH Hörn

Roermonder Str.

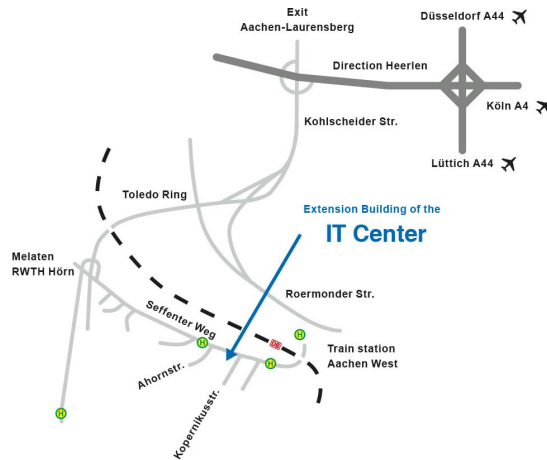Seffenter Weg

Train station Aachen West

Ahornstr.

Kopernikusstr.

BY CAR

From Cologne (A4) or Düsseldorf (A44) to the highway interchange "Aachener Kreuz", then A4 direction Netherlands, exit Aachen-Laurensberg. Turn right at the traffic lights, exit "Uniklinikum", then exit again "RWTH-Hörn", turn left, "Seffenter Weg", until you reach the junction with "Kopernikusstraße" (6th street).

BY PLANE

There are train connections from the airports of Düsseldorf (100 km), Cologne/ Bonn (85 km), Frankfurt (250 km) and Brussels (143 km).

BY TRAIN

The Aachen West train station is 10-minutes by foot from the IT Center.

BUS CONNECTIONS

The Bus route 3A connects the main station and the stop "Mies-van-der-Rohe-Straße" every 15 minutes. The Bus route 33 connects the city and the stop "Mies-van-der-Ro-he-Straße". To go back to city or main station please take bus route 3B (every 15 minutes).

Contact

Main building of the IT Center, Seffenter Weg 23, extension building on the left side, Kopernikusstraße 6.

POSTAL ADDRESS

IT Center
RWTH Aachen University
Seffenter Weg 23
52074 Aachen, Germany

Secretary

Tel.	+49 (0) 241. 80 – 29 10 0
Fax	+49 (0) 241. 80 – 22 24 1
E-Mail	verwaltung@itc.rwth-aachen.de

IT-ServiceDesk
Tel. +49 (0) 241 80 – 24 68 0

Online
IT Center www.itc.rwth-aachen.de

High Performance Computing (HPC)
www.itc.rwth-aachen.de/hpc

DIRECTOR
Prof. Dr. Matthias S. Müller

Parallel Programming in Computational Engineering & Science

March 16 - 20, 2015

PP
ces

Venue
IT Center

Kopernikusstraße 6
52074 Aachen

Sponsored by
BuLL

About the Event

This event will continue the tradition of previous annual week-long events that take place in Aachen every spring since 2001.

Throughout the week, we will cover parallel programming using MPI (Monday and Tuesday) and OpenMP (Wednesday and Thursday) in Fortran and C / C++ as well as performance tuning. Furthermore, we will introduce the participants to GPGPU programming with OpenACC (Friday). Hands-on exercises for each topic will be provided, which should not discourage you from working on your own code.

The topics are presented in a modular way, so that you could pick specific ones and register for the particular days only in order to let you invest your time as efficiently as possible.

Part I

Monday, March 16, 14:00– 17:30
Message Passing with MPI – Day I

Part II

Tuesday, March 17, 09:00 – 17:30
Message Passing with MPI – Day II

The Message Passing Interface (MPI) is the de-facto standard for programming large HPC clusters. We will introduce the basic concepts and give an overview of some advanced features. Also covered is hybrid parallelization, i.e. the combination of MPI and shared memory programming, which is gaining popularity as the number of cores per cluster node grows. Furthermore, we will introduce the TotalView debugger and a selection of performance and correctness tools (Score-P, Vampir, MUST).

Part III   Wednesday, March 18, 09:00 - 17:30
Shared Memory Programming with OpenMP – Day I

Part IV   Thursday, March 19, 09:00- 17:30
Shared Memory Programming with OpenMP – Day II

OpenMP is a widely used approach for programming shared memory architectures, supported by most compilers nowadays. We will cover the basics of the programming paradigm as well as some advanced topics such as programming NUMA machines. We will also cover a selection of performance and verification tools for OpenMP. The RWTH Compute Cluster comprises a large number of big SMP machines (up to 128 cores and 2 TB of main memory) as we consider shared memory programming a vital alternative for applications that cannot be easily parallelized with MPI. We also expect a growing number of application codes to combine MPI and OpenMP for clusters of nodes with a growing number of cores.

Furthermore, we will introduce the participants to modern features of the OpenMP 4.0 standard like vectorisation and programming for accelerators and for the Many Integrated Core (MIC) Architecture. Guest lectures and case studies complete these day's program.

Part V   Friday, March 20, 09:00 - 15:30
GPGPU Programming with OpenACC

OpenACC is a directive-based programming model for accelerators which enables delegating the responsibility for low-level (e.g. CUDA or OpenCL) programming tasks to the compiler. Using the OpenACC industry standard, the programmer can offload compute-intensive loops to an attached accelerator with little effort.
We will give an overview on OpenACC while focusing on NVIDIA GPUs. We will cover topics such as the GPU architecture, offloading loops, managing data movement between hosts and devices, tuning data movement, applying loop schedules and writing heterogeneous applications. We will also compare OpenACC to the newly introduced OpenMP directives for accelerators. Hands-on sessions are done on the RWTH Aachen GPU (Fermi) Cluster using PGI's OpenACC implementation.

Participants

Attendees should be comfortable with C/C++ or Fortran programming and interested in learning more about the technical details of application tuning and parallelization. The presentations will be given in English.

Costs

There is no seminar fee. All other costs (e.g. travel, hotel, and consumption) are at your own expenses.

Contact

Paul Kapinos
Tel.   +49 (0) 241. 80 - 24915
Fax / UMS   +49 (0) 241. 80 - 624915
E-Mail   hpcevent@itc.rwth-aachen.de

The PPCES event consists of five different parts. Please find further information, choose your topics of interest and register through our website by March 07, 2015
http://www.itc.rwth-aachen.de/ppces