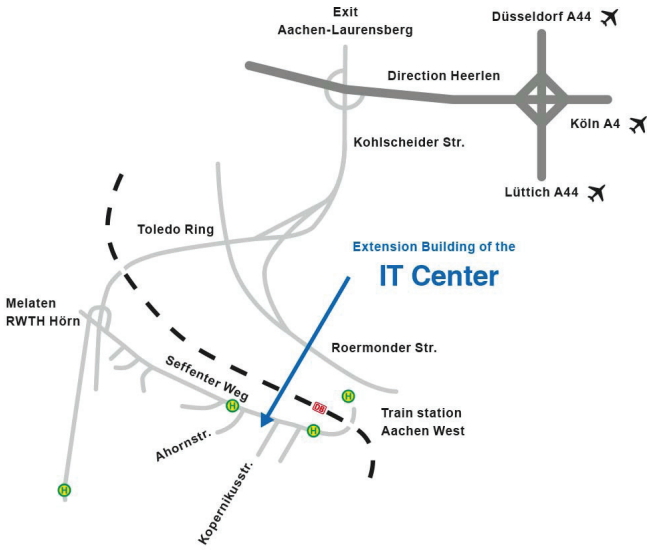
DIRECTIONS



BY CAR

From Cologne (A4) or Düsseldorf (A44) to the highway interchange ”Aachener Kreuz”, then A4 direction Netherlands, exit Aachen-Laurensberg. Turn right at the traffic lights, exit “Uniklinikum“, then exit again “RWTH-Hörn“, turn left, “Seffenter Weg“, until you reach the junction with “Kopernikusstraße” (6th street).

BY PLANE

There are train connections from the airports of Düsseldorf (100 km), Cologne/ Bonn (85 km), Frankfurt (250 km) and Brussels (143 km).

BY TRAIN

Aachen West train station to IT Center is a 10 minutes walk.

BUS CONNECTIONS

The Bus route 3A connects the main station and the stop “Mies-van-der-Rohe-Straße” every 15 minutes. The Bus route 33 connects the city and the stop “Mies-van-der-Rohe-Straße”. To go back to city or main station please take bus route 3B (every 15 minutes).

INFORMATION

www.aachen-tourist.de/en

CONTACT

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DIRECTOR

Prof. Dr. Matthias Müller

RWTH AACHEN UNIVERSITY

PARALLEL PROGRAMMING IN COMPUTATIONAL ENGINEERING & SCIENCE

March 10 - 14, 2014

PPCES

Venue
IT Center
Kopernikusstraße 6
52074 Aachen

Sponsored by

BULL

ABOUT THE EVENT

This event will continue the tradition of previous annual week-long events that take place in Aachen every spring since 2001.

Throughout the week we will cover a wide spectrum of topics, ranging from serial programming (Monday) to parallel programming using MPI (Tuesday) and OpenMP (Wednesday) in both Fortran and C/C++ as well as performance tuning. Furthermore, we will introduce the participants to modern features of the OpenMP standard like vectorization and programming for accelerators and for the Many Integrated Core (MIC) Architecture (Thursday) as well as GPGPU programming with OpenACC (Friday). Hands-on exercises for each topic will be provided, which should not discourage you from working on your own code.

The topics are presented in a modular way, so that you could pick specific ones and register for the particular days only in order to let you invest your time as efficiently as possible.

PART I **Monday, March 10, 14:00– 17:30**

Parallel Computing Architectures, Serial Tuning

After an introduction to the principles of today's parallel computing architectures, the configuration of the components of the RWTH Compute Cluster will be explained. As good serial performance is the basis for good parallel performance, we will cover basic serial tuning before introducing parallelization paradigms.

PART II **Tuesday, March 11, 09:00 – 17:30**

Message Passing with MPI

The Message Passing Interface (MPI) is the de-facto standard for programming large HPC clusters. We will introduce the basic concepts and give an overview of some advanced features. Also covered is hybrid parallelization, i.e. the combination of MPI and shared memory programming, which is gaining popularity as the number of cores per cluster node grows. Furthermore, we will introduce the TotalView debugger and a selection of performance tools.

PART III **Wednesday, March 12, 09:00 – 12:30**

Shared Memory Programming with OpenMP

OpenMP is a widely used approach for programming shared memory architectures, supported by most compilers nowadays. We will cover the basics of the programming paradigm as well as some advanced topics such as programming NUMA machines. We will also cover a selection of performance and verification tools for OpenMP. The RWTH Compute Cluster comprises a large number of big SMP machines (up to 128 cores and 2 TB of main memory) as we consider shared memory programming a vital alternative for applications that cannot be easily parallelized with MPI. We also expect a growing number of application codes to combine MPI and OpenMP for clusters of nodes with a growing number of cores.

PART IV **Thursday, March 13, 09:00 – 17:30**

OpenMP Programming for the MIC Architecture

The Intel Xeon Phi coprocessor is based on the Intel Many Integrated Core (MIC) architecture and can be programmed with standard techniques like OpenMP, POSIX threads and MPI. We will give a brief introduction to this new architecture and demonstrate the different programming possibilities. Then we will introduce the new OpenMP features for programming accelerators and for vectorization. The OpenMP programming tools are essential for finding and debugging errors and will be presented in the last talk that day.
For the labs you can continue working on the provided lab exercises or get started with porting or tuning your own codes. Don't put your expectations too high though as time for working on nontrivial codes is limited. The better you are prepared, the more you will profit from this opportunity.

PART V **Friday, March 14, 09:00 – 15:30**

GPGPU Programming with OpenACC

OpenACC is a directive-based programming model for accelerators which enables delegating the responsibility for low-level (e.g. CUDA or OpenCL) programming tasks to the compiler. Using the OpenACC industry standard, the programmer can offload compute-intensive loops to an attached accelerator with little effort.
We will give an overview on OpenACC while focusing on NVIDIA GPUs. We will cover topics such as the GPU architecture, offloading loops, managing data movement between hosts and devices, tuning data movement, applying loop schedules and writing heterogeneous applications. We will also compare OpenACC to the newly introduced OpenMP directives for accelerators. Hands-on sessions are done on the RWTH Aachen GPU (Fermi) Cluster using PGI's OpenACC implementation.

Participants

Attendees should be comfortable with C/C++ or Fortran programming and interested in learning more about the technical details of application tuning and parallelization. The presentations will be given in English.

Costs

There is no seminar fee. All other costs (e.g. travel, hotel, and consumption) are at your own expenses.

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The PPCES event consists of five different parts.
Please find further information, choose your topics of interest and register through our website by
March 03, 2014

http://www.rz.rwth-aachen.de/ppces