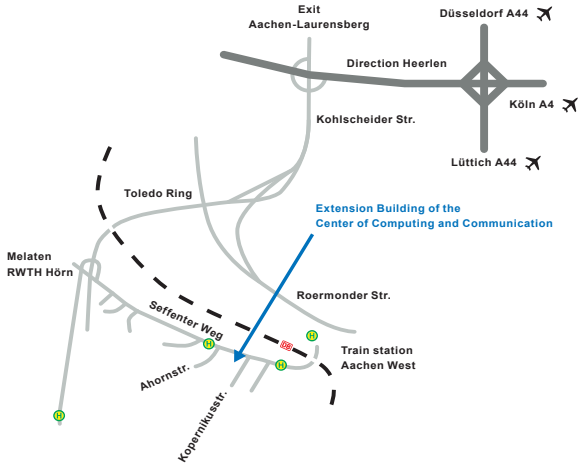
DIRECTIONS



BY CAR

From Cologne (A4) or Düsseldorf (A44) to the highway interchange ”Aachener Kreuz”, then A4 direction Netherlands, exit Aachen-Laurensberg. Turn right at the traffic lights, exit “Klinikum“, then exit again “RWTH-Hörn“, turn left, “Seffenter Weg“, until you reach the junction with “Kopernikusstraße” (6th street).

BY PLANE

There are train connections from the airports of Düsseldorf (90 km), Cologne (85 km), Frankfurt (250 km) and Brussels (143 km).

BY TRAIN

The train station Aachen West is a 10-minutes walk to the Center.

BUS CONNECTIONS

The Bus route 3A connects the main station and the stop “Mies-van-der-Rohe-Straße” every 15 minutes. The Bus route 33 connects the city and the stop “Mies-van-der-Rohe-Straße”. To go back to city or main station please take bus route 3B (every 15 minutes).

INFORMATION

www.aachen-tourist.de/en

CONTACT

Main building of the Center for Computing and Communication, Seffenter Weg 23, with the new extension building on the left side, Kopernikusstraße 6.

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ACTING DIRECTOR

Prof. Dr. Matthias Müller

RWTH AACHEN UNIVERSITY

PARALLEL PROGRAMMING IN COMPUTATIONAL ENGINEERING & SCIENCE

March 11 - 15, 2013

PPCES

Venue

Kopernikusstraße 6
52074 Aachen

Sponsored by

ABOUT THE EVENT

This event will continue the tradition of previous annual week-long events taking place in Aachen every spring since 2001.

Throughout the week, we will cover serial (Monday) and parallel programming using MPI (Tuesday) and OpenMP (Wednesday) in Fortran and C/C++ as well as performance tuning addressing both Linux and Windows platforms. Furthermore, we will introduce the participants to GPGPU programming (Thursday) and provide ample opportunities for hands-on exercises including a „bring-your-own-code“ session on Friday.

These topics are presented in a modular way, so that you can choose, pick and register for single days in order to let you invest your time as efficiently as possible.

PART I **Monday, March 11, 14:00– 17:30**

Introduction, Parallel Computing Architectures, Serial Tuning

After an introduction to the principles of today‘s parallel computing architectures, the configuration of the new components of the RWTH Compute Cluster delivered by the company Bull will be explained. As good serial performance is the basis for good parallel performance, we cover serial tuning before introducing parallelization paradigms.

PART II **Tuesday, March 12, 09:00 – 17:30**

Message Passing with MPI

The Message Passing Interface (MPI) is the de-facto standard for programming large HPC Clusters. We will introduce the basic concepts and give an overview of some advanced features. Furthermore, we will introduce the TotalView debugger and a selection of performance tools. We will also cover hybrid parallelization, i.e. the combination of MPI and shared memory programming. Hybrid parallelization is gaining popularity as the number of cores per cluster node is growing.

PART III **Thursday, March 14, 09:00 – 17:30**

GPGPU Programming with OpenACC

We will study GPU programming as a parallel programming skill. We will briefly introduce GPU architectures and explain why GPU programming differs from multicore parallel programming. CUDA is NVIDIA‘s architecture for executing highly parallel applications on their GPUs; we will introduce NVIDIA‘s CUDA C extensions in comparison with the OpenCL standard, showing basic concepts, performance measurement and tuning. Then, we will look at the PGI Accelerator Model, a directive-based approach to program GPUs and give a glimpse into the upcoming OpenACC programming paradigm for accelerators.

PART IV **Wednesday, March 13, 09:00 – 12:30**

Shared Memory Programming with OpenMP

OpenMP is a widely used approach for programming shared memory architectures, which is supported by most compilers nowadays. We will cover the basics of the programming paradigm as well as some advanced topics, such as programming NUMA machines or clusters, coherently coupled with the vSMP software from ScaleMP. We will also cover a selection of performance and verification tools for OpenMP. The RWTH Compute Cluster comprises a large number of big SMP machines (up to 128 cores and 2 TB of main memory) as we consider shared memory programming a vital alternative for applications which cannot be easily parallelized with MPI. We also expect a growing number of application codes to combine MPI and OpenMP for clusters of nodes with a growing number of cores.

PART V **Friday, March 15, 09:00 – 15:00**

Lab Exercises, Tune your own Code

At the end of a week full of presentations and hands-on sessions, we would like to give you the opportunity to dive into some more practical details, to continue working on lab exercises or to get started with porting or tuning your own codes. Don‘t put your expectations too high though, as time for working on large codes is limited. You will profit more from this opportunity the better you are prepared.

Participants

Attendees should be comfortable with C/C++ or Fortran programming and interested in learning more about the technical details of application tuning and parallelization. The presentations will be given in English.

- There will be two additional short introductory courses on the specifics of the software environment of the RWTH Compute Cluster for local users on Wednesday, March 7 at 9 am (Windows) and Wednesday, March 14 at 9 am (Linux).

Costs

There is no seminar fee. All other costs (e.g. travel, hotel, and consumption) are at your own expenses.

Contact

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The PPCES event consists of five different parts.
Please find further information, choose your topics of interest and register through our website by
March 04, 2013:

http://www.rz.rwth-aachen.de/ppces