RWTH AACHEN UNIVERSITY

RWTH Aachen University
Center for Computing and Communication

March 19 – 23, 2012

Parallel Programming for Computational Engineering & Science
Introduction

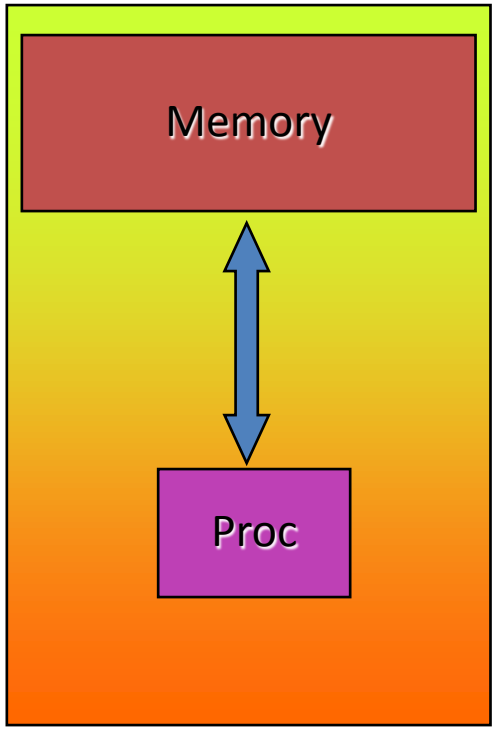
Dieter an Mey

Kindly sponsered by

PPCES 2009

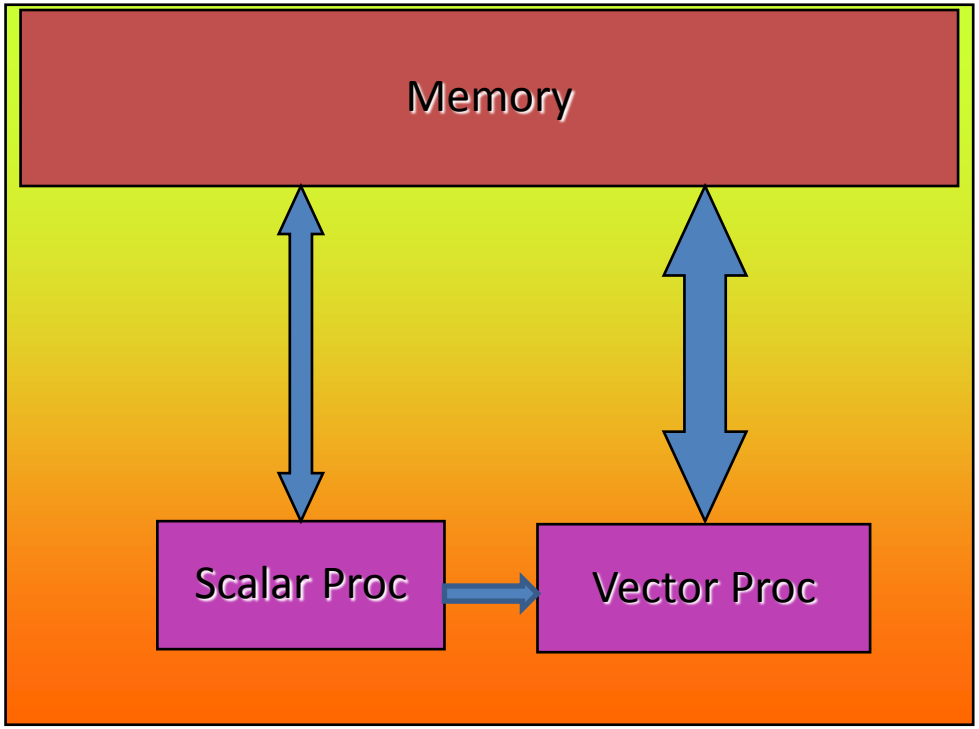
PPCES 2012

The Programmer‘s Naive Perspective



1976
CDC Cyber 175
7(?) Mflop/s
40 MHz
3,3 MB memory

Vector Computers



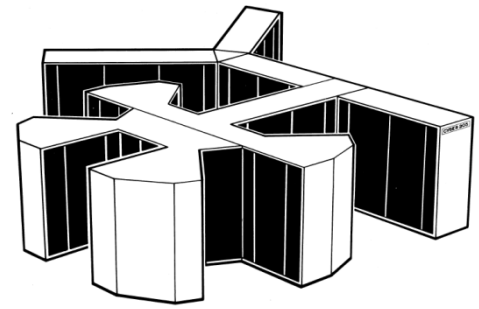


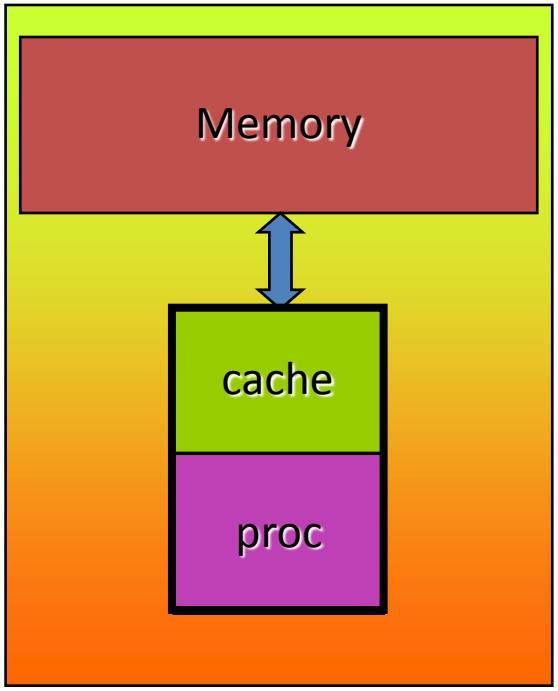
Figure 1-1. CYBER 205 Central Computer (Series 400)

```
DO I = 1, 65535
    A(I) = B(I) + X * C(I)
END DO
```

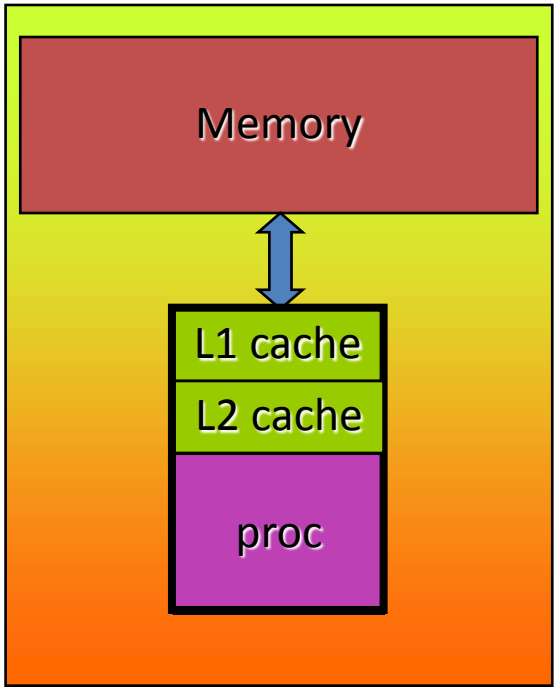
1982
CDC Cyber 205 in Bochum
50 MHz
200 Mflop/s

1990
SNI S600/20
(Fujitsu VP2600)
5 Gflop/s
1 GBy memory

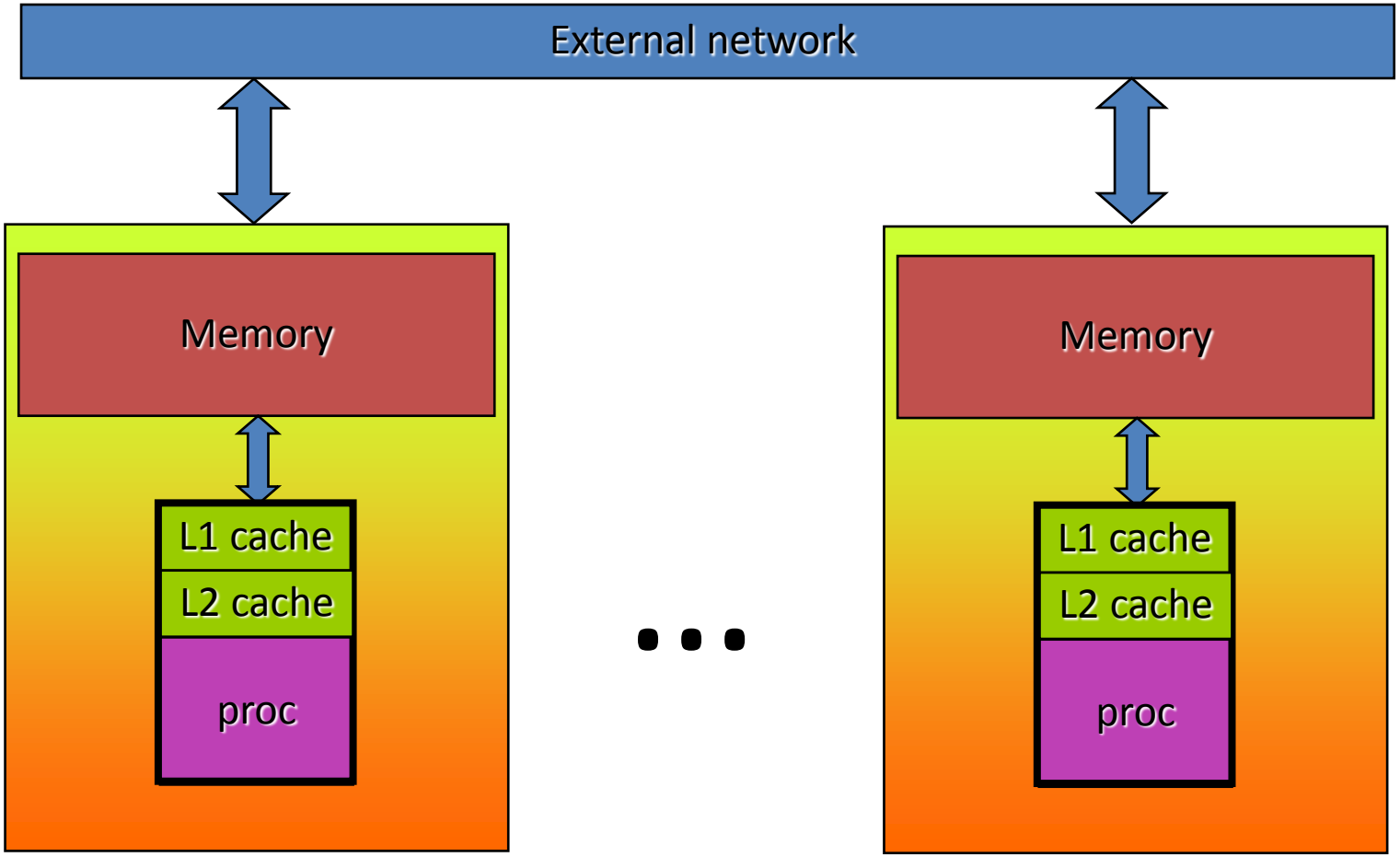
Microprocessors with a Cache



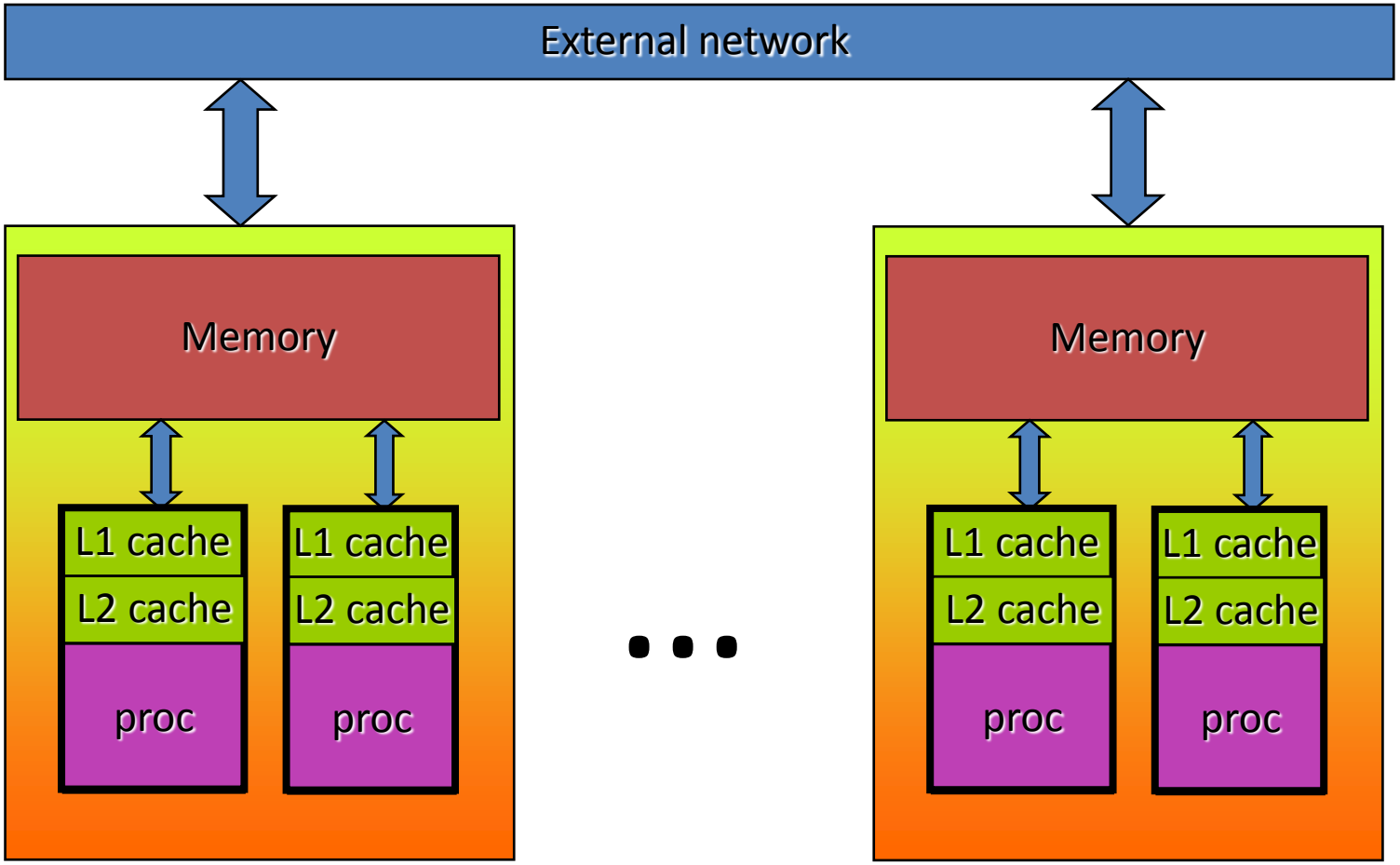
Multiple Cache Levels



(Beowulf-) Clusters

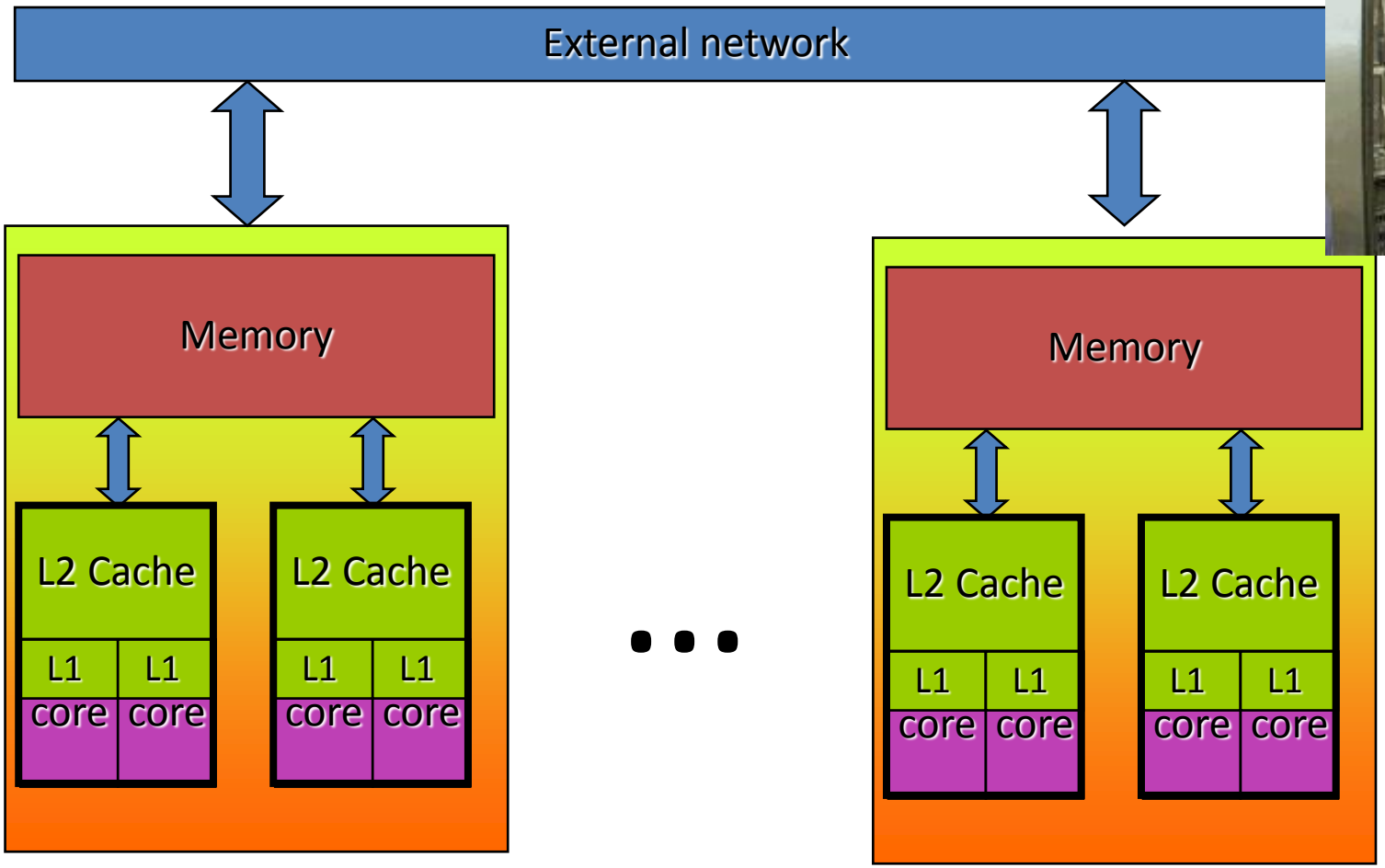


Multiprocessors with Shared Memory



1999:
Fujitsu-Siemens
hpcLine
16 nodes each
2 Pentium III
600 MHz
512 MB memory
SCI 2D-torus

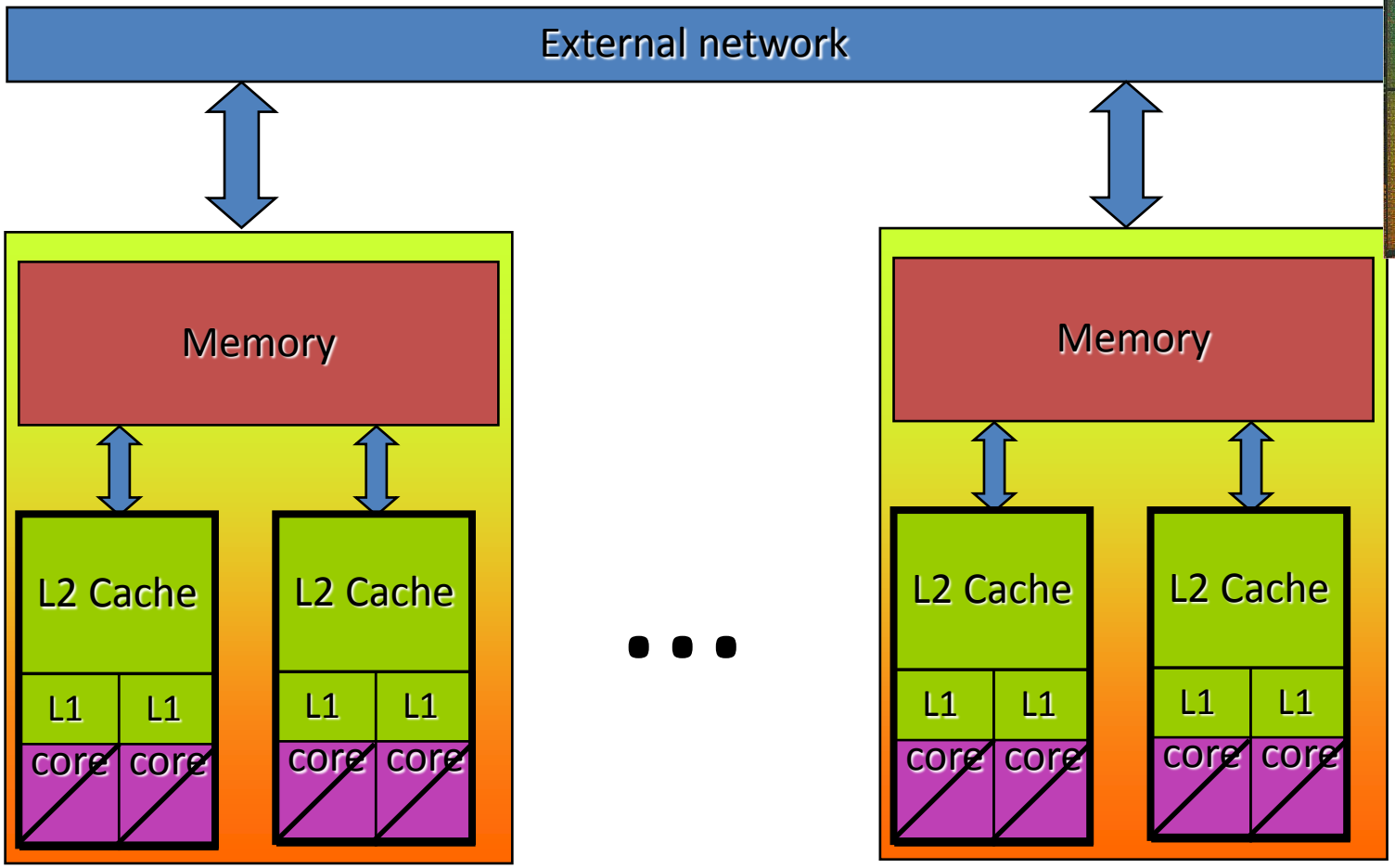
Multiple Multicore Processors

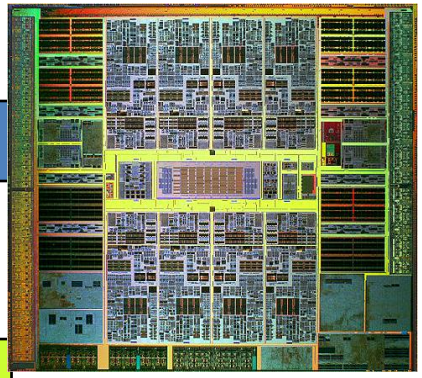


2004
4 nodes
Sun Fire 25K
72 UltraSPARC IV
2 cores
1,05 GHz
288 GB memory

16 nodes
Sun Fire 6900
24 UltraSPARC IV
2 cores
1,2 GHz
96GB memory
Sun Fire Link

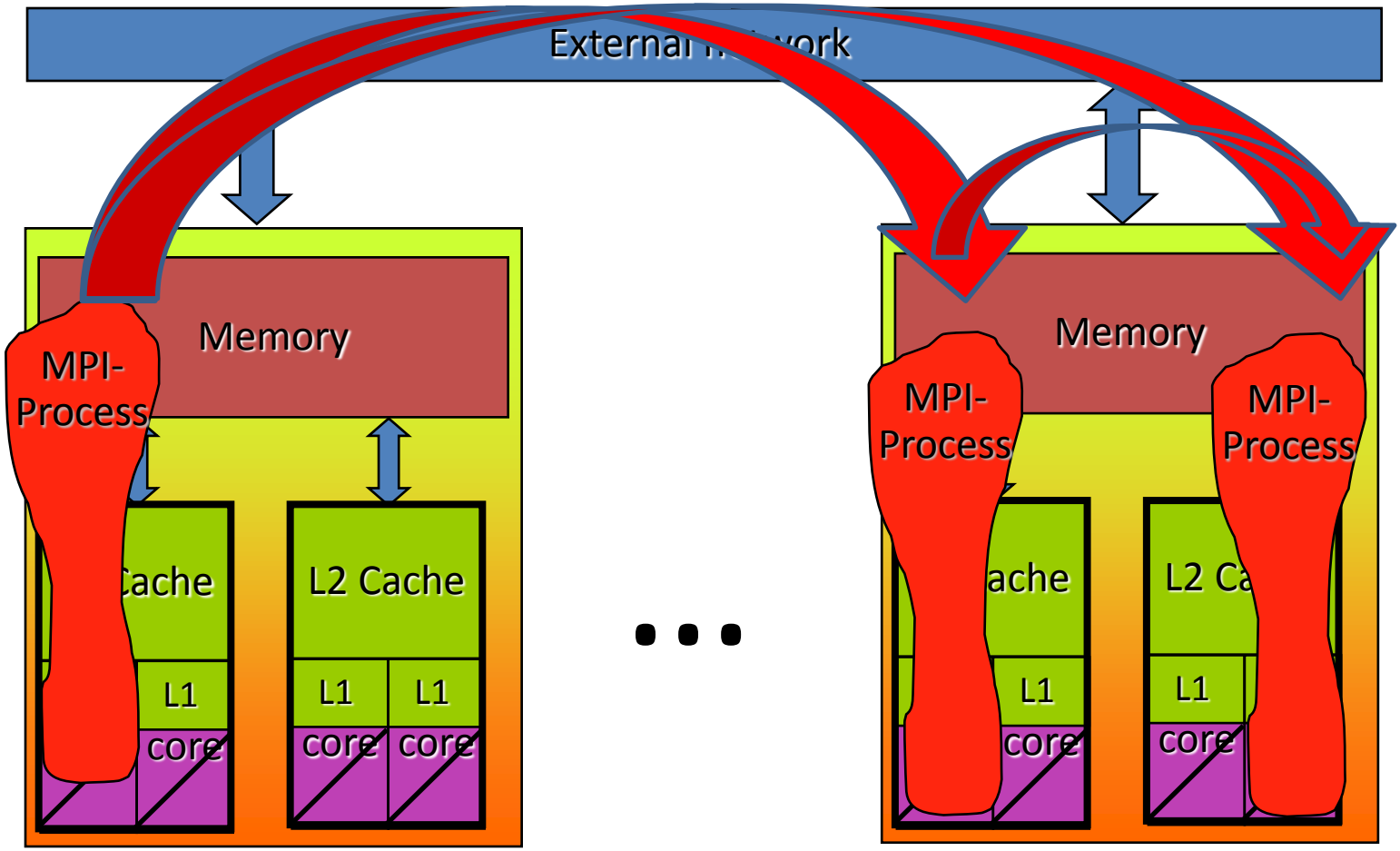
Chip Multi-Threading



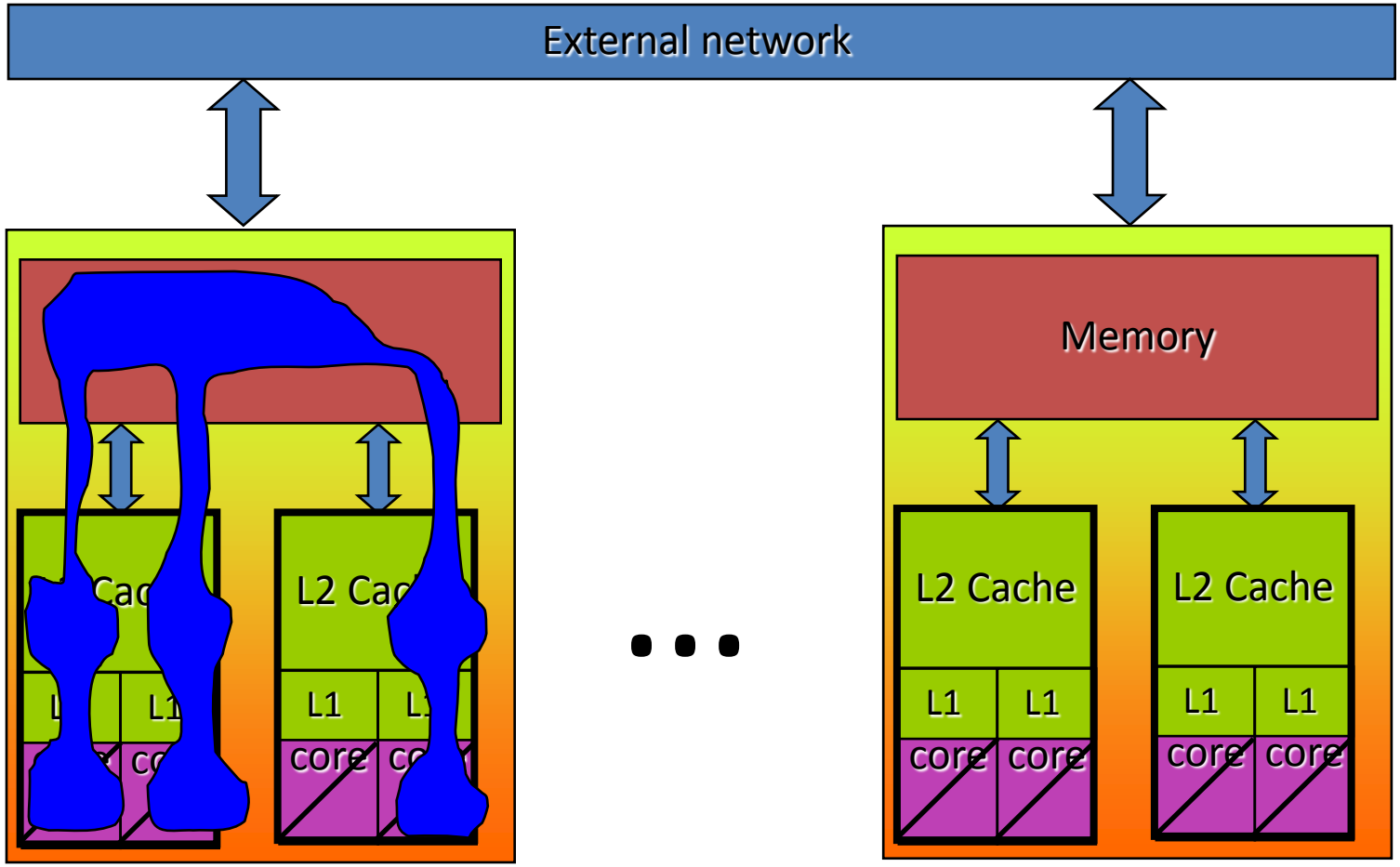


2007
20 nodes
Sun Fire T2000
1 UltraSPARC T2
„Niagara 2“
8 cores
8 threads
1,4 GHz
32GB memory
Infiniband

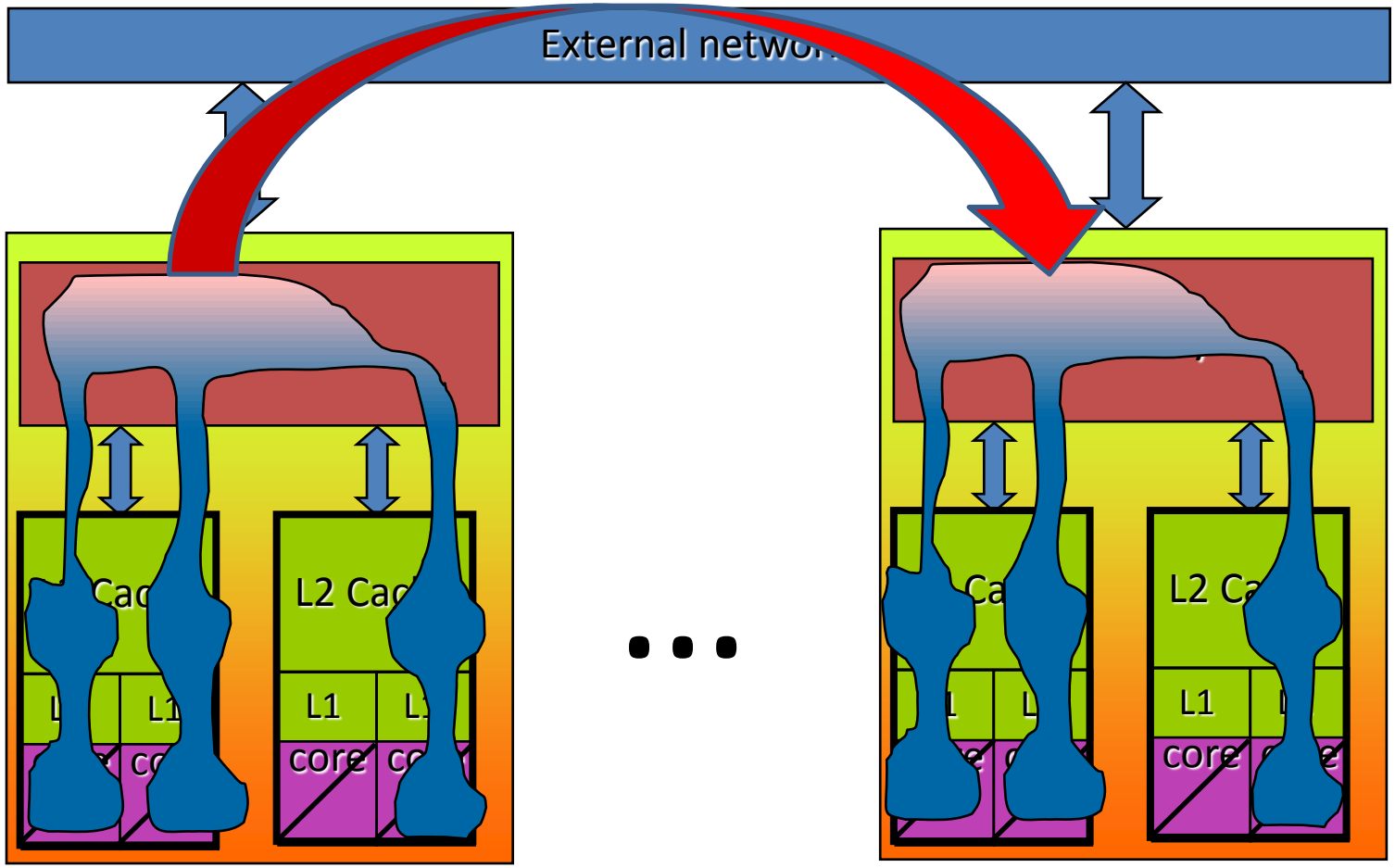
Message Passing with MPI



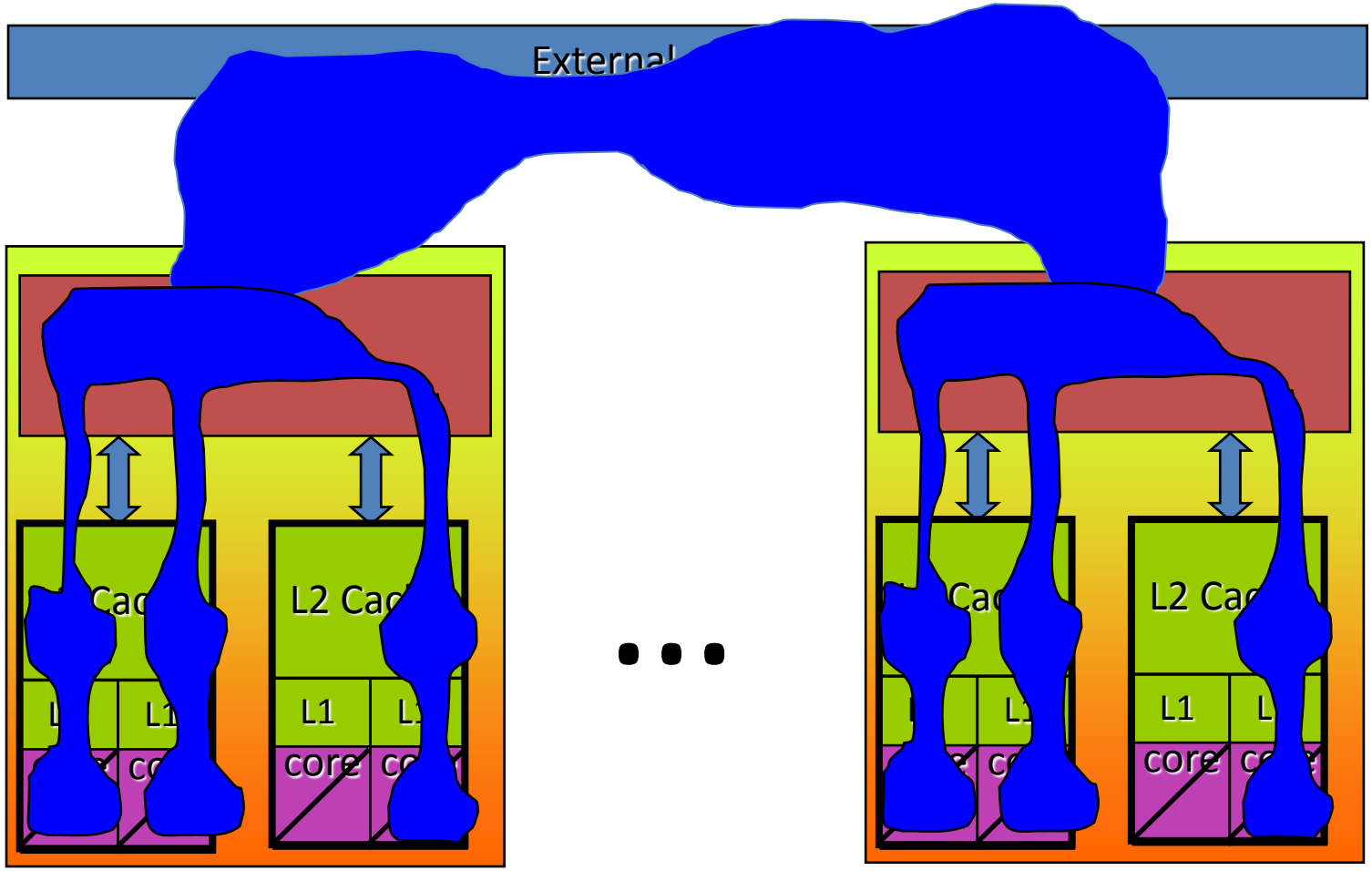
Shared Memory Programming with OpenMP



MPI + OpenMP = Hybrid Parallelization

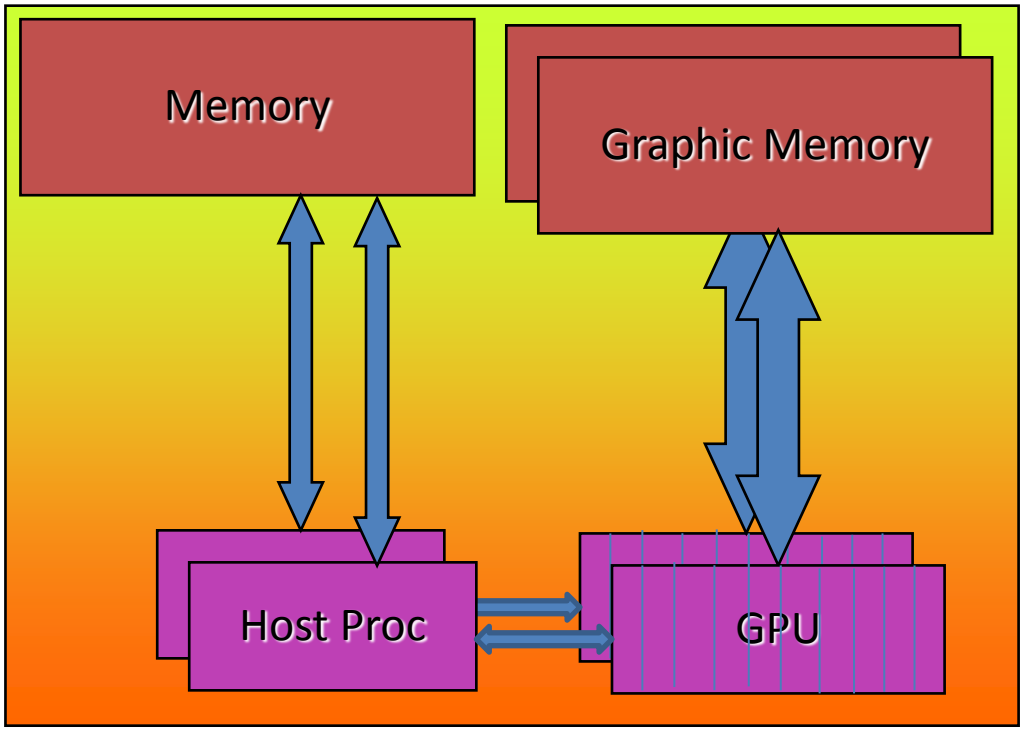


Virtual Shared Memory Programming with OpenMP (using Software from ScaleMP)



How to deal with this Complexity?

… and then there are GPGPUs …



2011:
28 (+1) Nodes
2 Intel Xeon Westmere
+
2 NVIDIA Quadro 6000
515.2 GFLop/s
6 GB memory

```
!$acc region do copyin(b,x,c) copyout(a)
  DO I = 1, 65535
      A(I) = B(I) + X * C(I)
  END DO
```

PPCES Overview

Part I **Monday, March 19, 14-17:30**	**Processor Architectures and Serial Programming**
Part II **Tuesday, March 20, 9-17:30**	**Message Passing with MPI**
Part III **Wednesday, March 21, 9-17:30**	**Shared Memory Programming with OpenMP**
Part IV **Thursday, March 22, 9-17:30**	**GPGPU Programming**
Part V **Friday, March 23, 9-12:30**	**Labs + Code Tuning**