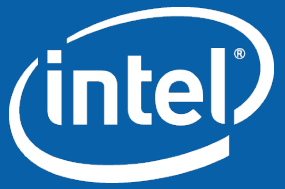


Intel® Array Building Blocks

Dr.-Ing. Michael Klemm
Sen. Application Engineer
Software and Services Group

Legal Disclaimer

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS OTHERWISE AGREED IN WRITING BY INTEL, THE INTEL PRODUCTS ARE NOT DESIGNED NOR INTENDED FOR ANY APPLICATION IN WHICH THE FAILURE OF THE INTEL PRODUCT COULD CREATE A SITUATION WHERE PERSONAL INJURY OR DEATH MAY OCCUR.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or go to: http://www.intel.com/design/literature.htm

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Optimization Notice

Optimization Notice

Intel® compilers, associated libraries and associated development tools may include or utilize options that optimize for instruction sets that are available in both Intel® and non-Intel microprocessors (for example SIMD instruction sets), but do not optimize equally for non-Intel microprocessors. In addition, certain compiler options for Intel compilers, including some that are not specific to Intel micro-architecture, are reserved for Intel microprocessors. For a detailed description of Intel compiler options, including the instruction sets and specific microprocessors they implicate, please refer to the "Intel® Compiler User and Reference Guides" under "Compiler Options." Many library routines that are part of Intel® compiler products are more highly optimized for Intel microprocessors than for other microprocessors. While the compilers and libraries in Intel® compiler products offer optimizations for both Intel and Intel-compatible microprocessors, depending on the options you select, your code and other factors, you likely will get extra performance on Intel microprocessors.

Intel® compilers, associated libraries and associated development tools may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include Intel® Streaming SIMD Extensions 2 (Intel® SSE2), Intel® Streaming SIMD Extensions 3 (Intel® SSE3), and Supplemental Streaming SIMD Extensions 3 (Intel® SSSE3) instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors.

While Intel believes our compilers and libraries are excellent choices to assist in obtaining the best performance on Intel® and non-Intel microprocessors, Intel recommends that you evaluate other compilers and libraries to determine which best meet your requirements. We hope to win your business by striving to offer the best performance of any compiler or library; please let us know if you find we do not.

Notice revision #20101101

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Agenda – Day 1

09:00am	Introduction to Intel® Array Building Blocks (ArBB)
10:30am	Break
10:45am	Introduction to Intel® Array Building Blocks (ArBB)
12:00pm	Lunch
02:00pm	Hands-on
03:30pm	Break
03:30pm	Hands-on
04:45pm	Wrap-up of Day 1
05:00pm	End of Day 1

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

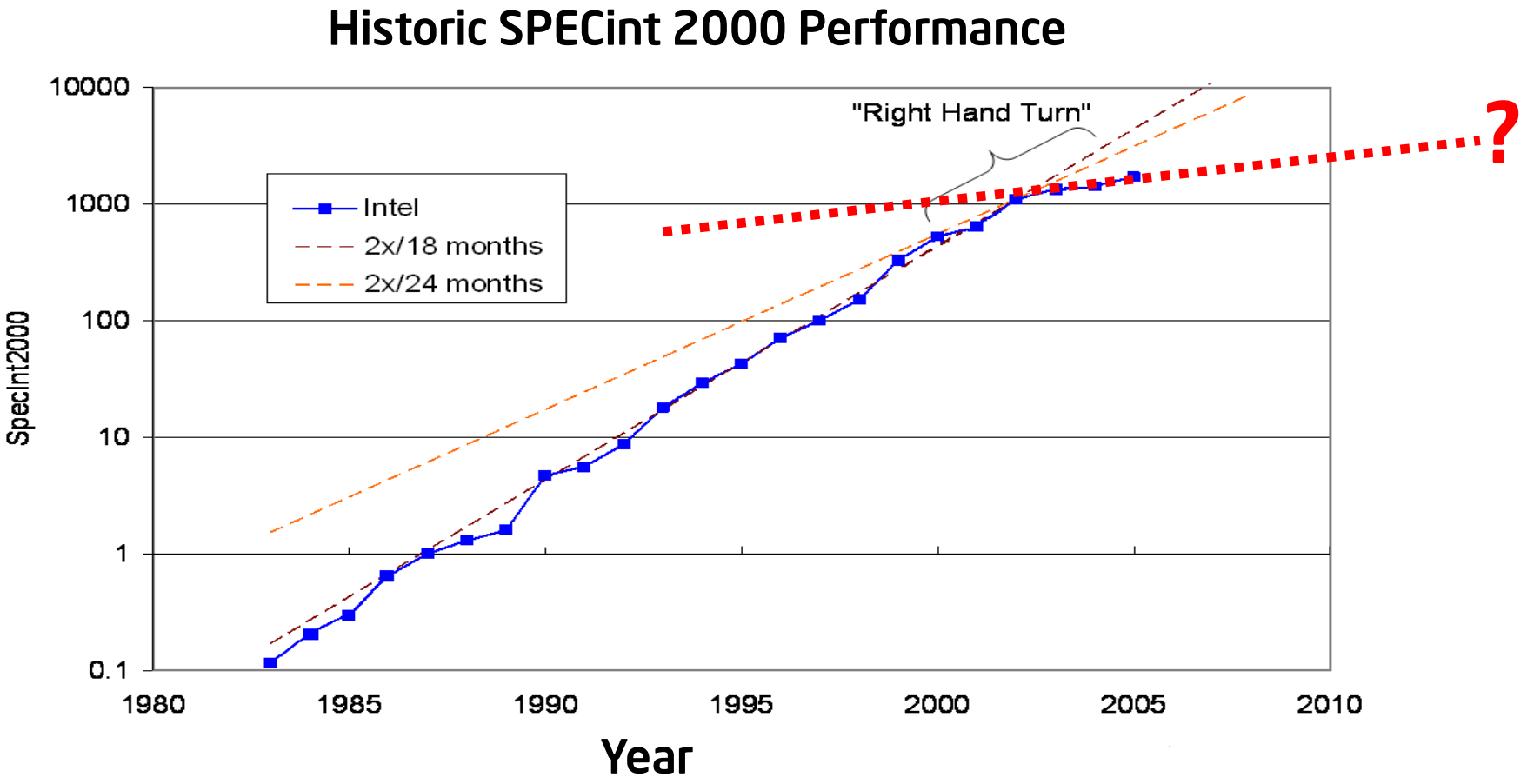
Agenda – Day 2

09:00am	ArBB Execution Engine
10:30am	Break
10:45am	ArBB Advanced Programming
12:00pm	Lunch
02:00pm	Hands-on
03:15pm	Wrap-up of Day 2
03:30pm	End of Day 2

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

We've seen this slide before (2008)

Is performance at a plateau?



Source: published SPECInt data

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Aggressive Performance Ramp

- A sample of points on the Graph!
- Nieuport* 17 C.1 fighter of World War I
- Upgrade for 1973: Dassault* Mirage F1
- Upgrade for 2012: Dassault* nEUROn

Source: Photos from Wikipedia.org

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

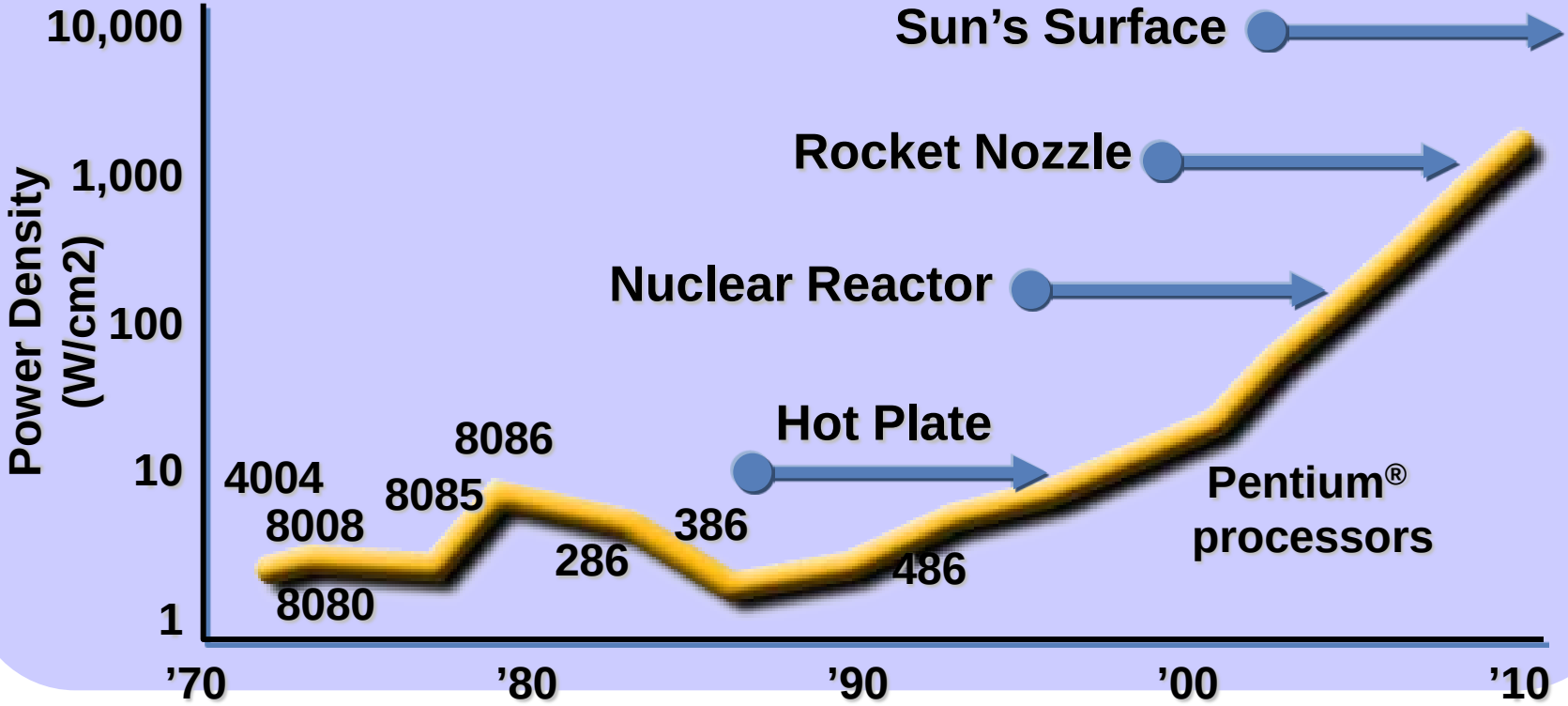
Technological plateaus…

Cessna* 172, 1956 model

Cessna* 172, 2009 model

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

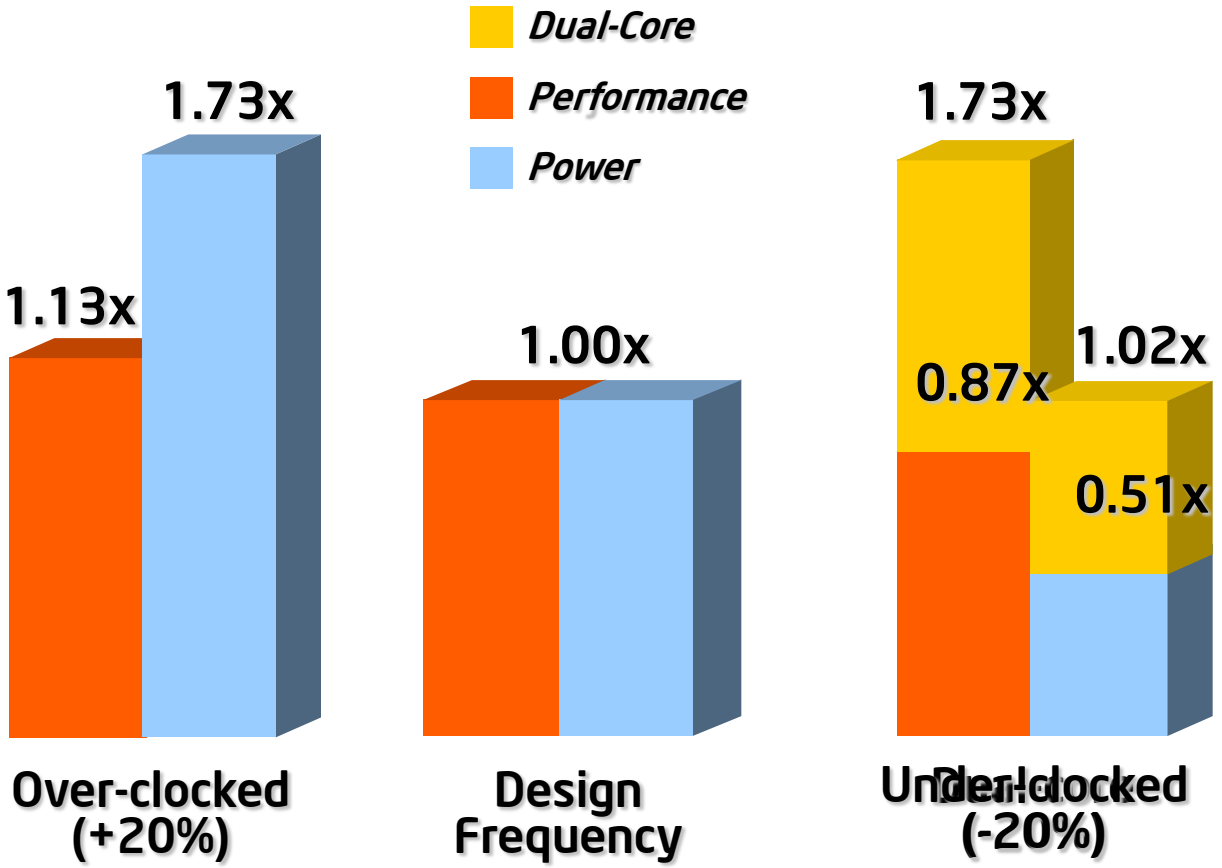
Why is *everyone* going multi-core?



Power Density Race

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

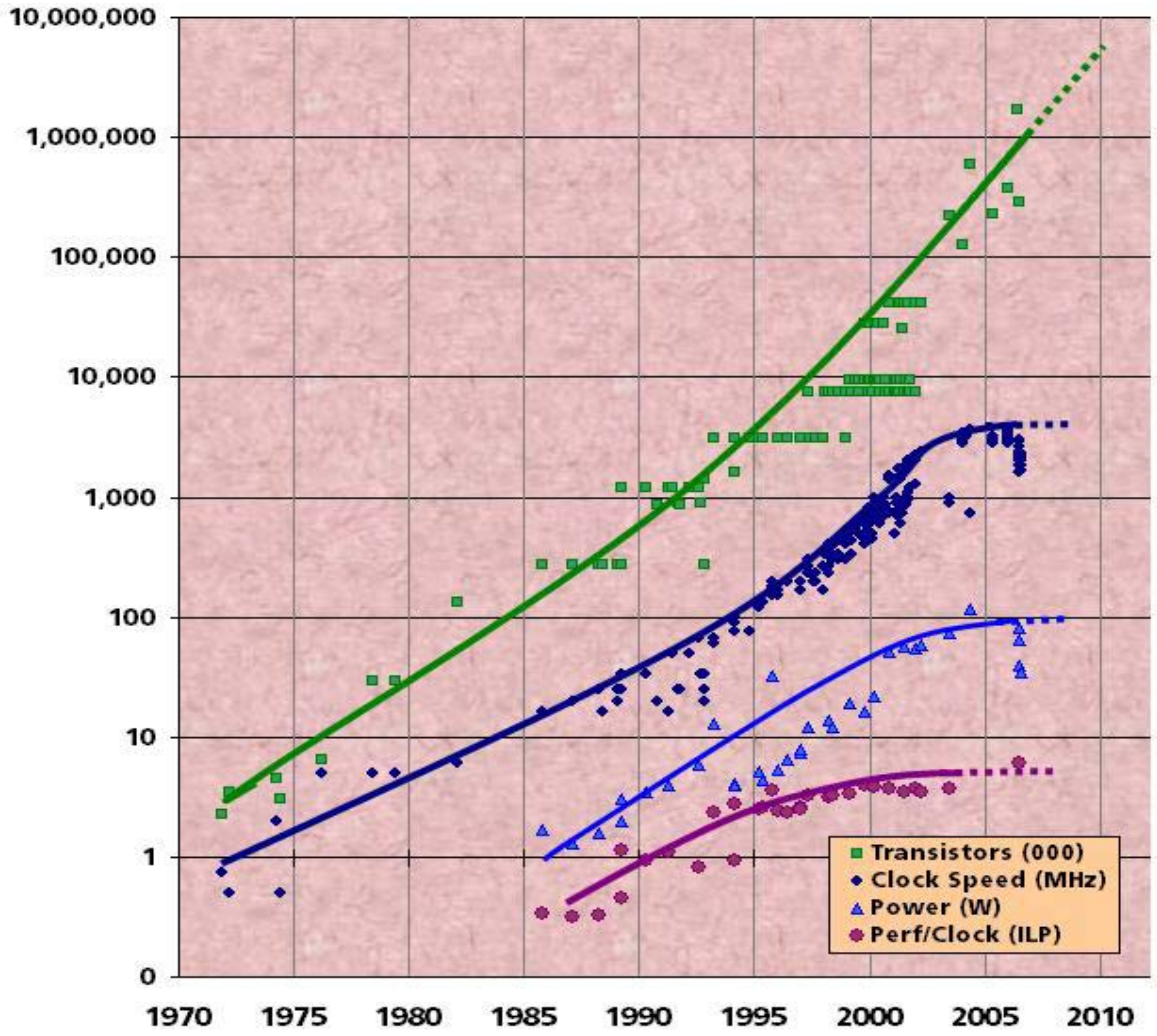
Multicore
beating the *power/performance* barrier



Relative single-core frequency and Vcc

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Moore's Law Reinterpreted



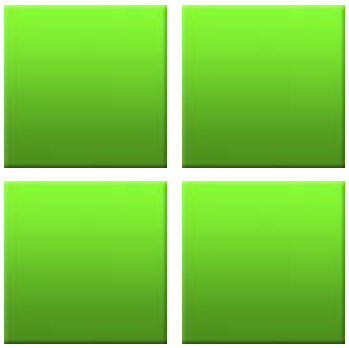
- Clock frequency no longer increasing
- Speed no longer increasing at former pace
- Number of transistors still growing
- Number of cores rather than clock speed is doubling every 18 months

From K. Olukotun, L. Hammond, H. Sutter, and B. Smith

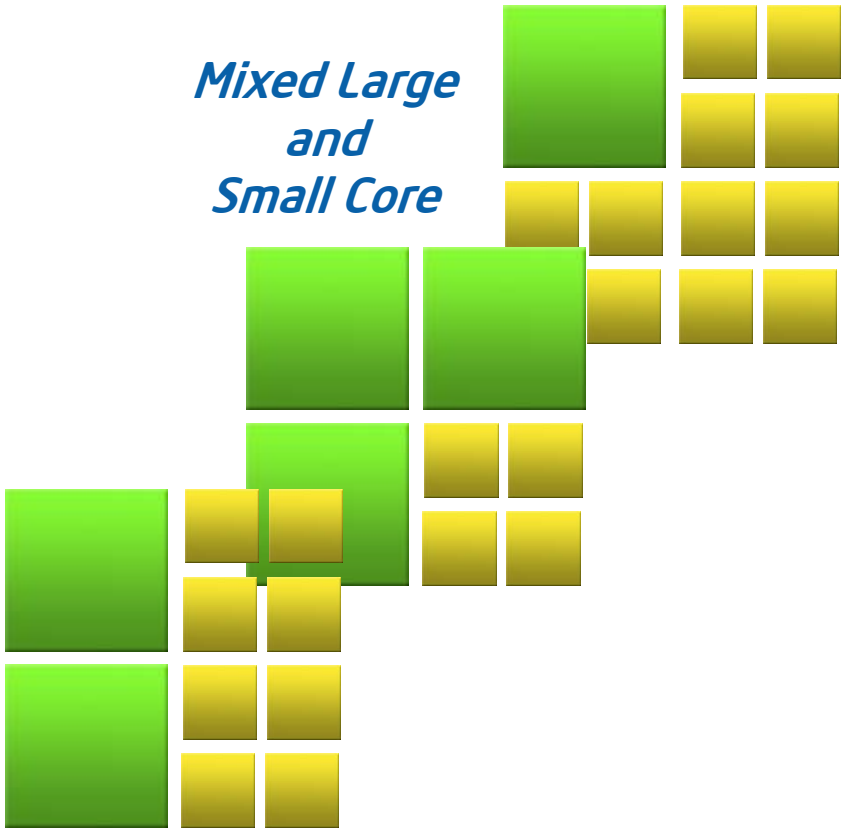
Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Future: Multicore and Manycore

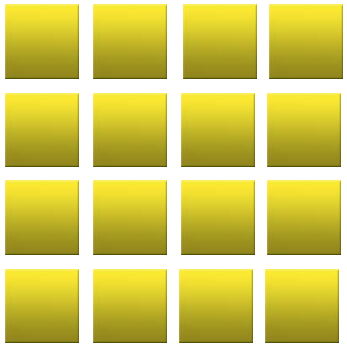
All Large Core



Mixed Large and Small Core



All Small Core

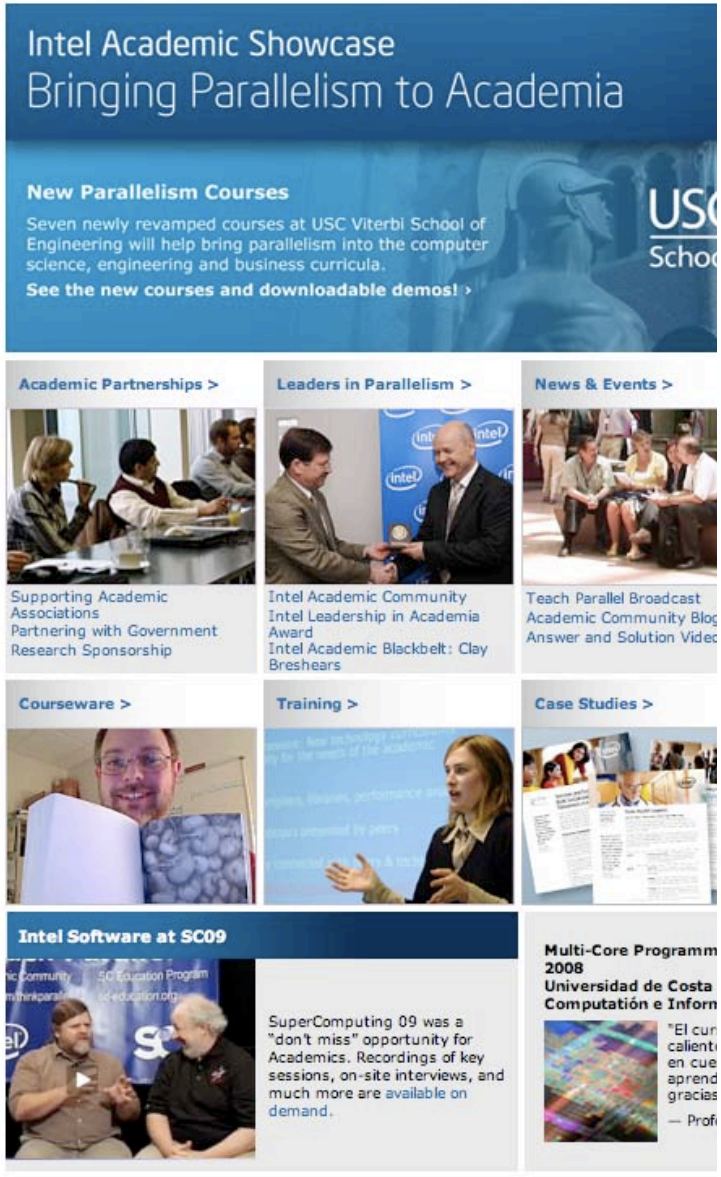


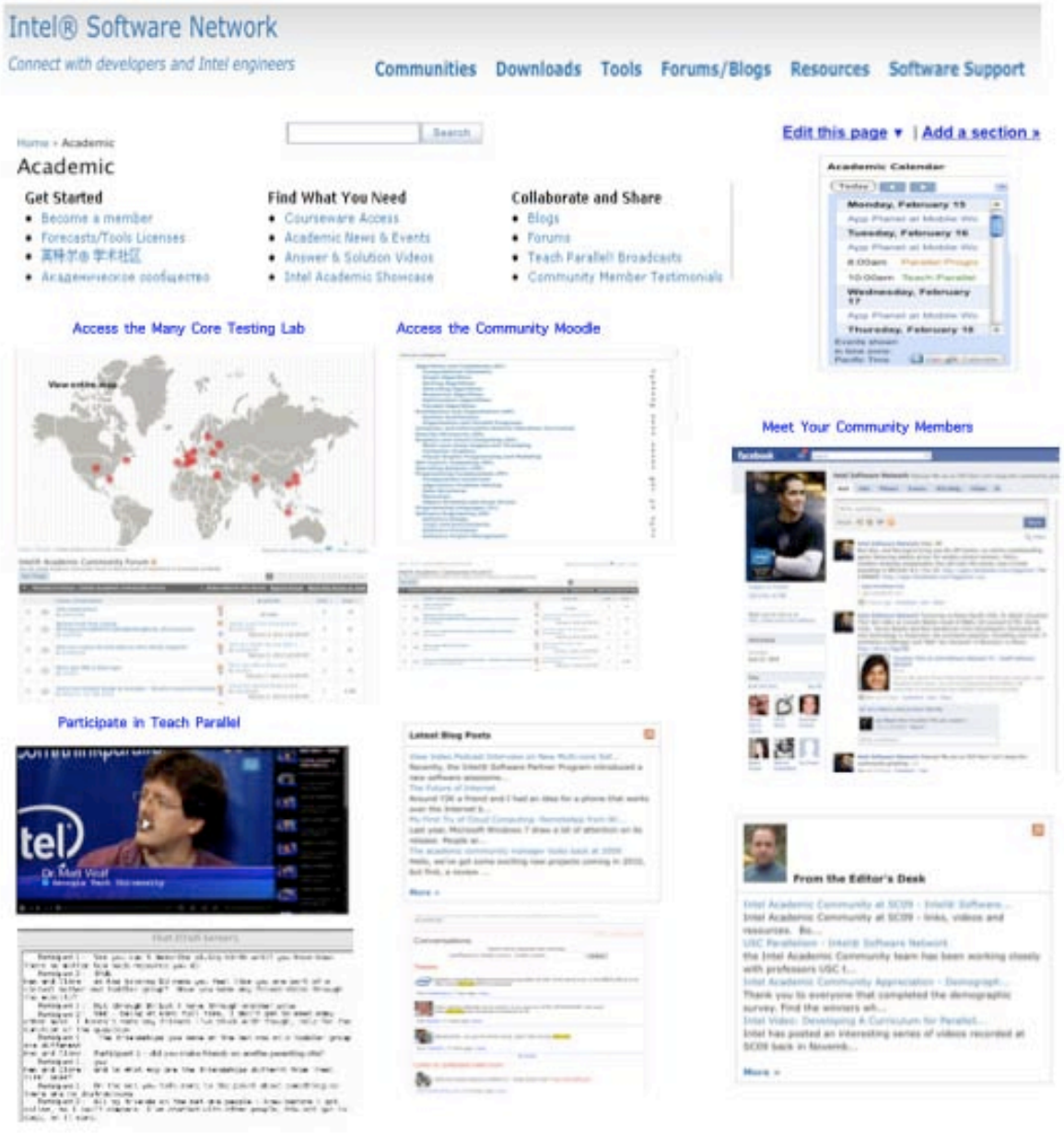
Connections to memory bank(s), connections between processors, memory coherency models – all come into play. Diversity!

Note: the above pictures do not necessarily represent any current or future Intel products

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Online Resources – Intel Academic Community



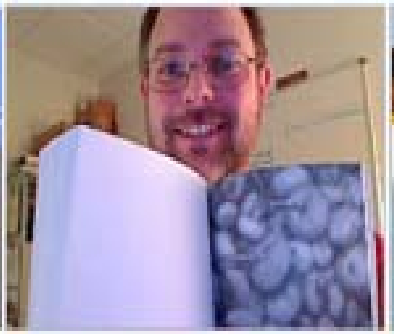


What is the Intel Academic Community?

- A program to engage university computer sciences professors and departments to prepare students for modern and future Intel technologies, especially parallel computing and manycore.
- We provide an online community, content resources, forums, tools, scaling platforms, curriculum standards, publications etc.
- We partner with governments, top tier university professors, academic curriculum advisory bodies, and Intel Corporate Affairs to build influence and lead curriculum development worldwide.

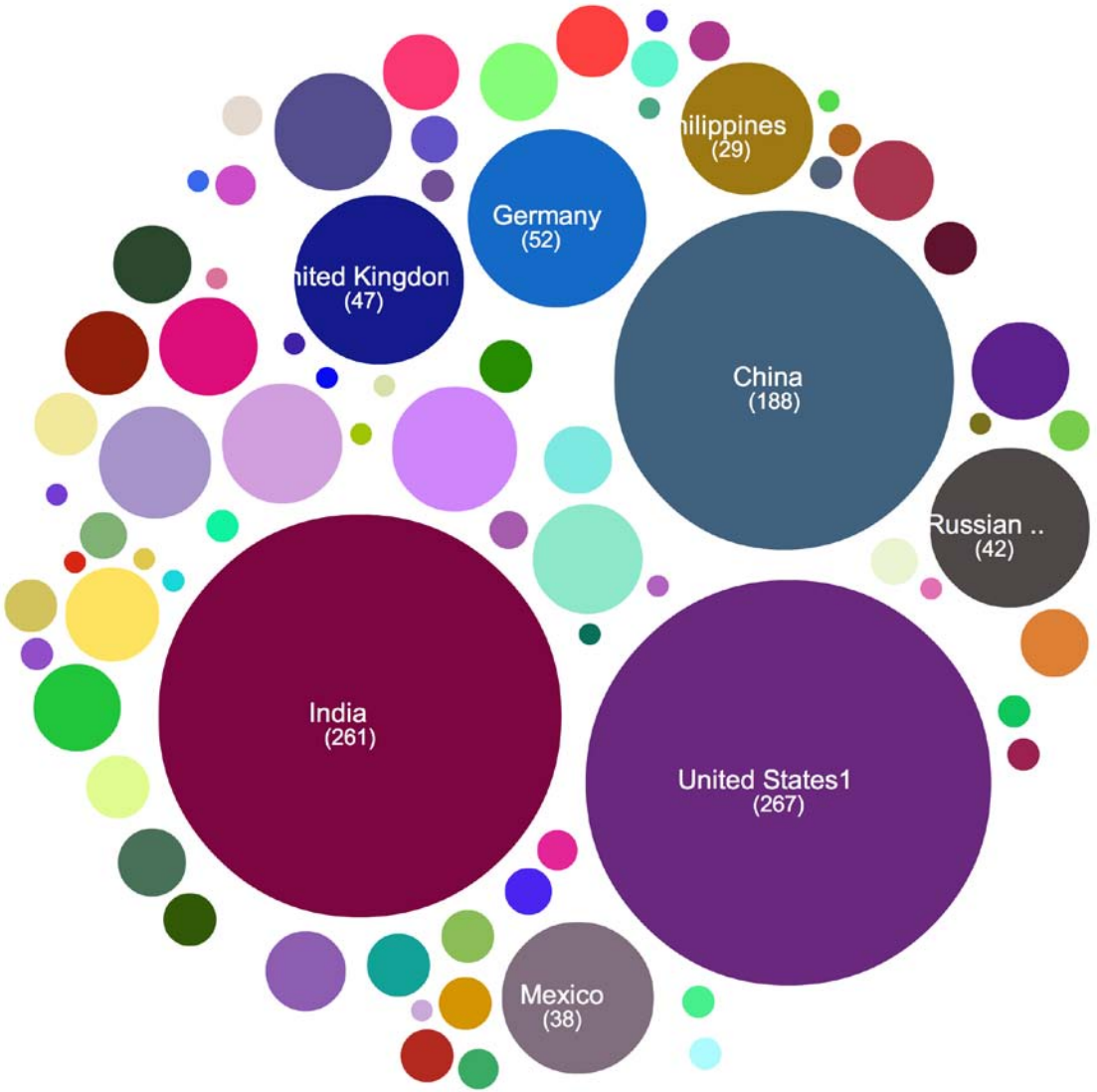
http://intel.com/thinkparallel





Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Membership in Intel Academic Community



Implementing parallel computing into CS curriculum

85% outside USA

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Community Outreach

Teach Parallel on Intel Software Network TV

Options: Edit

Watch our latest broadcast

Common Strategies fo
Parallelism.

Professor Wen-mei Hw
("Jerry") Sanders III-
Micro Devices Endowe
Electrical and Comput
Engineering in the Co
Science Laboratory of
University of Illinois at
Champaign.

Curriculum for Multi-c

Professor Matt Wolf, R
Scientist CERCS Cente
Experimental Research in
Computer Systems.

into the entry classes, and getting increasingly more focused as
means we have to forgo teaching some things to make space in
been surprisingly little.
See this episode here.

The View from Intel Research.

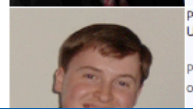
Dr. Tim Mattson, Intel Principal
Engineer.

Dr. Tim Mattson, Intel Principal Engineer, has been an early (an
parallel both in industry and academia. His past work as creator
research on abstractions that bridge across parallel system des
environments, and application software give him a unique persp
parallelism.
See this episode here.

Re-envisioning the Computer
Science Curriculum.

Dr. Dan Reed, Microsoft, Director
of Multicore Research.

Dan Reed is Microsoft's Scalable and Multicore Computing Strat
talks about how industry and academia must change to cope w
heterogeneous compute cores.



Preparing Students for
Ubiquitous Parallelism.

Professor Daniel Ernst, University
of Wisconsin, Eau Claire.

Professor Ernst has successfully introduced parallelism through
UWEC. His approach is to give students practice with the conce
early and often by integrating them into existing course work. J
See this episode here.

accessing the list on the player above or
talk below.

en, MIT
Parallel Mat

Dr. Joel Adams, Dept of Computer Science, Calvin College.

on, Intel
ineer.
tern
nd Parallel
Computing.

Jason Arviso, Navajo Technical College, Internet to the Hogan.

Dr. John Gustafson. He's not just a scientist, he's a law!

Dr. David O'Hallaron, Intel Labs Pittsburgh & Carnegie Mellon University. Open Cirrus Cloud Computing Project.

Dr. Jesse Bemley, JEF -The Joint Educational Foundation.

Dr. Matt Wolf, Research Scientist CERCS Center for Experimental Research in Computer Systems.

Dr. James Reinders, Intel Chief Software Evangelist.

Todd Rosenquist, Sr. Technical Consulting Engineer, Intel® Math Kernel Library

Skylar Thompson, Parallel Octave, Bootable Cluster CD.

Dr. Paul McKenney, Distinguished Engineer at IBM Linux Technology Center

Dr. Robert M. Panoff, founder and Executive Director of The Shodor Education

Werner Krotz-Vogel, Technical Marketing Engineer at Intel for Intel® Cluster Tools

Dr. Julie Mullen, MIT Lincoln Lab. Parallel Mat Lab.

Dr. Rebecca Hartman- Baker, Oak Ridge Natioanl Lab. Women in Computing.

The Intel Academic Community introduces...

The Manycore Testing Lab

Cloud computing on 32-cores for academia

Industry demands the best...

- Bring a 32-core development environment directly into your classrooms, labs, or research facilities, for free!
- Give your students an edge — the opportunity to learn from an industry leader and gain practical experience with the latest technologies.
- Test and validate the scalability of your labs, publish your results with Intel, and do your part to advance computational sciences.

*Visit the **Intel booth** for the first ever, hands-on demo of the Manycore Testing Lab. Learn how you can transform your curriculum with remote access to the latest manycore technologies.*

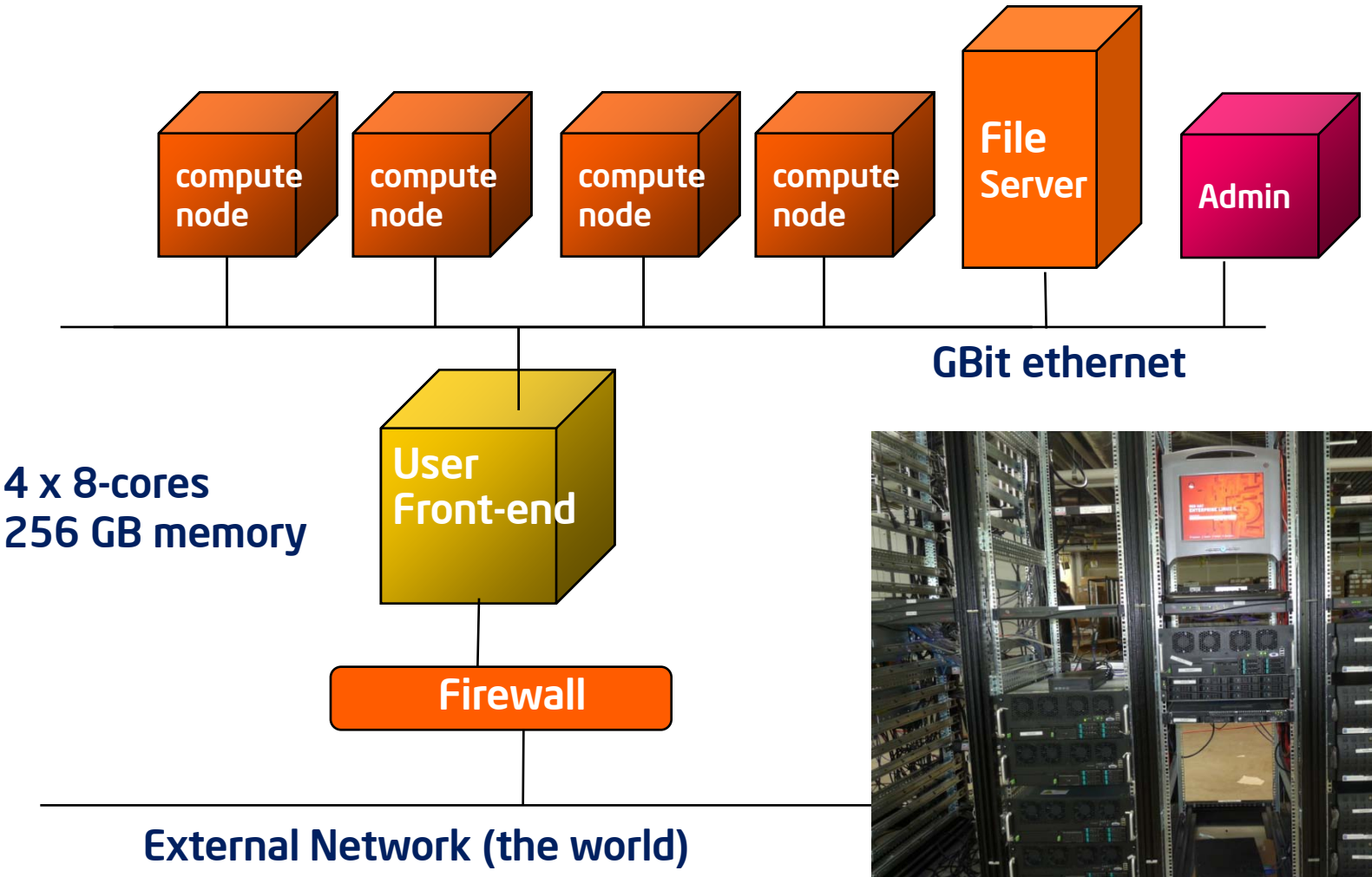
Visit Us @ www.intel.com/software/academic

Can your students compete?

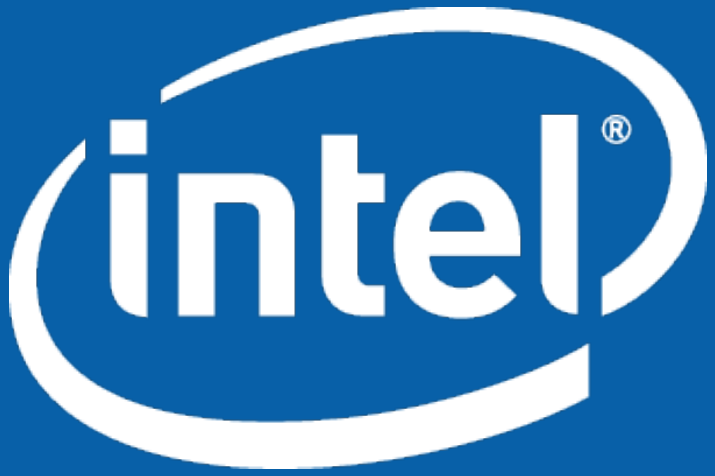
Will they be prepared for a business world where manycore processors and parallel programming are ubiquitous?

Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.

Manycore Testing Lab Configuration



Copyright © 2010, Intel Corporation. All rights reserved.
*Other brands and names are the property of their respective owners.


intel