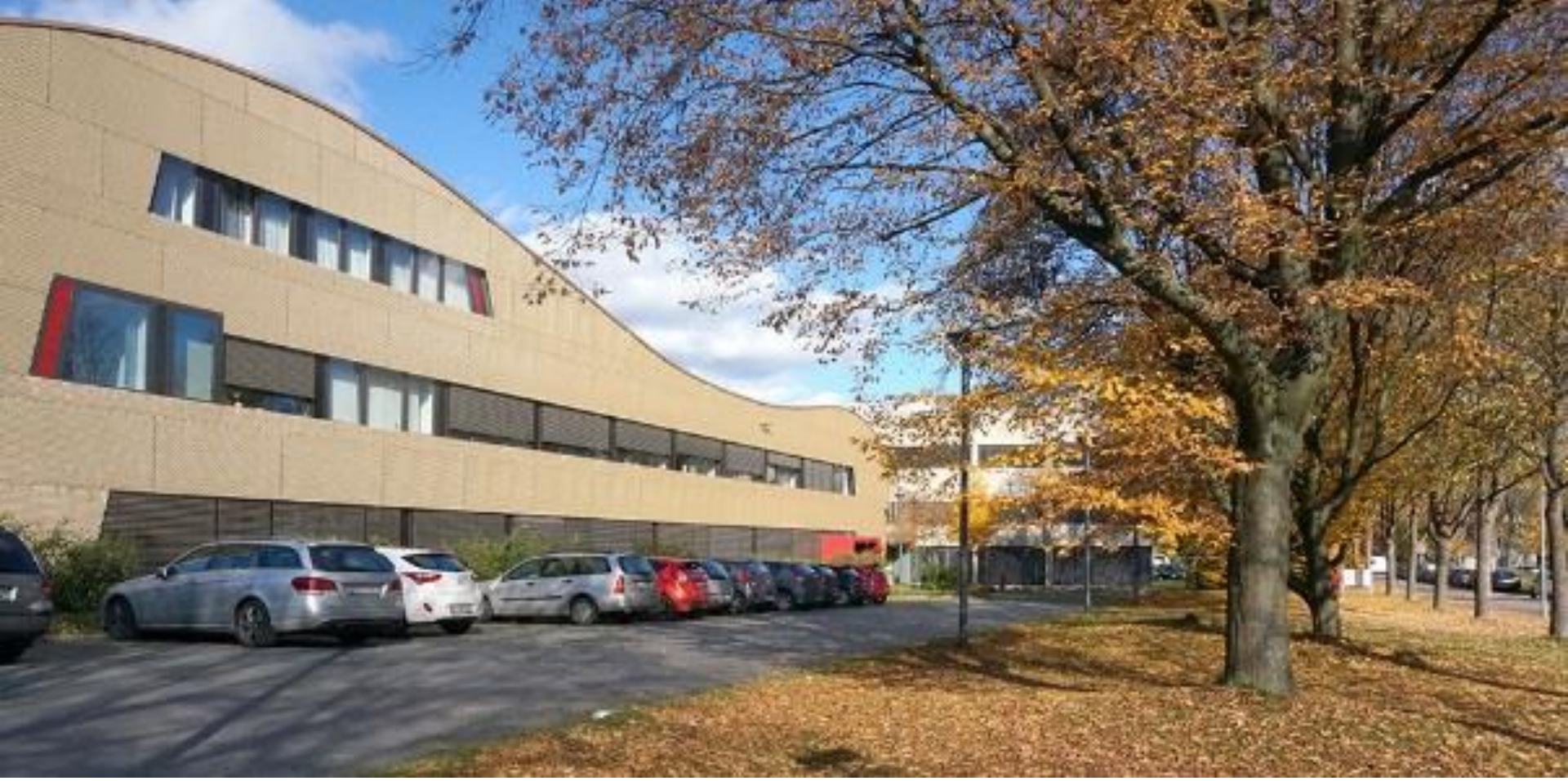


aiXcelerate 2018

Dr. Sandra Wienke
IT Center, RWTH Aachen University

IT Center | RWTH AACHEN UNIVERSITY

Concept

- Presentations
  - Participation open for all cluster users
  - Short introduction of CLAIX-2018 and new software environment
  - Performance analysis and optimization on new hardware

- Tuning workshop
  - Closed session
  - Bring your own code
  - Lightning talks: presentation of codes before and after the tuning workshop

- Sponsors

CLAIX-2018

CLAIX-2018 – Procurement

- Evaluation
  - Focus on economic viability of real-world application → RWTH Job-Mix
  - Total cost of ownership metrics: hardware acquisition costs, energy consumption, cooling costs, job-mix performance

- Schedule
  - July 2018: Announcement of winner → NEC
  - October 2018: Installation start of CLAIX-2018
  - November/ December 2018: testing and acceptance stage
  - December 2018: production

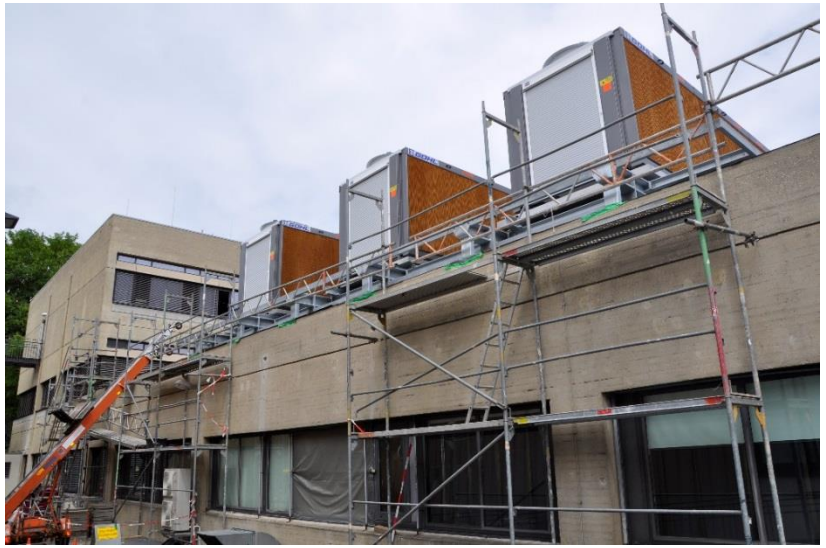
CLAIX-2018: Compute Nodes & Performance

- **1032 MPI nodes**
  - 2 Intel Xeon Platinum 8160 CPUs (Skylake)
  - 24 cores per CPU (→ 48 cores/ 96 hyper threads per node)
  - 2.1 GHz, 3.7 GHz turbo mode
  - 2 x AVX512 FMA
  - 192 GB main memory
  - Local SSD: 480 GB
- **48 MPI-GPU nodes**
  - MPI nodes with two NVIDIA V100 SXM2 GPUs
  - GPU-GPU interconnect: NVLink technology

- Performance
  - Theoretical peak: 3.55 PFlops
  - Job-Mix: average performance per core increases by 30% for the same data input sets (compared to CLAIX-2016)

CLAIX-2018: Network, Storage & Cooling

- Network
  - Intel Omni-Path 100G fabric
- Storage
  - New Lustre-based solution
  - Also accessible from compute nodes of CLAIX-2016
  - Capacity: 10 PB
  - Read/write bandwidth: 150 GB/s
- Cooling
  - Racks: NEC side cooler solution
  - Inlet water: 30°C
  - Free cooling



Cooling towers (construction phase)

CLAIX-2018: Extension

- Tier-3 system
- 215 MPI nodes
- 6 MPI-GPU nodes
- Expected to be in operation in January 2019

Speaker

- Intel
  - M. Klemm
  - C. Dahnken

- RRZE
  - T. Gruber

- RWTH
  - M. Wagner
  - P. Kapinos
  - J. Hahnfeld

Agenda

	Mon, Dec 3, 2018		Tue, Dec 4, 2018		Wed, Dec 5, 2018
		9:00-10:30	Hands-on BYOC, continued (RWTH & Intel)	9:00-10:30	Hands-on BYOC (RWTH & Intel)
10:30-11:00	Registration / Coffee	10:30-11:00	Coffee Break	10:30-11:00	Coffee Break
11:00-13:00	Workshop & Cluster Intro (RWTH, 45min) Skylake Microarchitecture (Intel, 75min)	11:00-13:00	likwid (RRZE, 60min) VTune Amplifier (Intel, 60min)	11:00-13:00	Hands-on BYOC (RWTH & Intel)
13:00-14:00	lunch	13:00-14:00	lunch	12:30-14:00	lunch
14:00-15:00	SIMD Programming and SKX Performance Considerations (Intel)	14:00-15:30	Hands-on BYOC: perf tools (RWTH & Intel)	14:00-14:30	App Lightn. Talks (attendees)
				14:30-15:30	Hands-on BYOC (RWTH & Intel)
15:00-15:30	Coffee Break				
15:30-16:00	App Lightn. Talks (attendees)	15:30-16:00	Coffee Break	15:30-15:45	Coffee Break
16:00-18:00	Hands-on BYOC: compile code, analyze compiler reports (RWTH & Intel)	16:00-18:00	Hands-on BYOC: perf tools (RWTH & Intel)	16:00-17:00	Hands-on BYOC (RWTH & Intel)
		19:00	Social Dinner Restaurant Palladion		